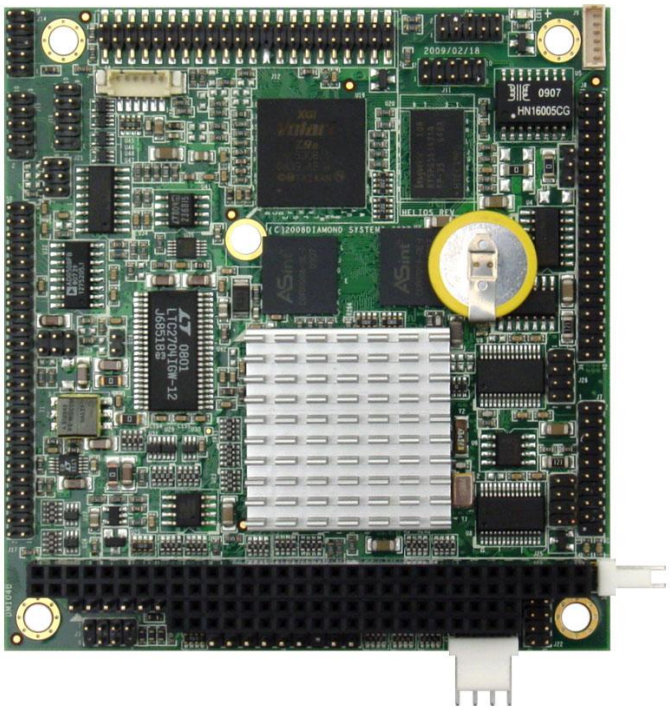
HELIOS SINGLE BOARD COMPUTER

PC/104 SBC with Vortex Processor
and Integrated Data Acquisition

Rev B9: January 2016



Revision	Date	Comment
B	5/15/2009	Major update
B1-8	2/23/2012	Minor corrections; removed 300MHz models
B9	1/4/2016	Updated power consumption

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1. IMPORTANT SAFE HANDLING INFORMATION

WARNING!

ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

The Helios board contains a high number of I/O connectors with connection to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor's) embedded computer boards.

ESD damage – This type of damage is usually almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board eventually simply stops working, because some component becomes defective. Usually the failure can be identified and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage during handling or storage – On some boards we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

Power supply wired backwards – Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply (i.e. almost all ICs). In this case the board will most likely will be unrepairable and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. **Check twice before applying power!**

Board not installed properly in PC/104 stack – A common error is to install a PC/104 board accidentally shifted by 1 row or 1 column. If the board is installed incorrectly, it is possible for power and ground signals on the bus to make contact with the wrong pins on the board, which can damage the board. For example, this can damage components attached to the data bus, because it puts the ±12V power supply lines directly on data bus lines.

Overvoltage on analog input – If a voltage applied to an analog input exceeds the design specification of the board, the input multiplexor and/or parts behind it can be damaged. Most of our boards will withstand an erroneous connection of up to ±35V on the analog inputs, even when the board is powered off, but not all boards, and not in all conditions.

Overvoltage on analog output – If an analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most of our boards, a short circuit to ground on an analog output will not cause trouble.

Overvoltage on digital I/O line – If a digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and the damage could even extend past that chip to others in the circuit.

Bent connector pins – This type of problem is often only a cosmetic issue and is easily fixed by bending the pins back to their proper shape one at a time with needle-nose pliers. The most common cause of bent connector pins is when a PC/104 board is pulled off the stack by rocking it back and forth left to right, from one end of the connector to the other. As the board is rocked back and forth it pulls out suddenly, and the pins at the end get bent significantly. The same situation can occur when pulling a ribbon cable off of a pin header. If the pins are bent too severely, bending them back can cause them to weaken unacceptably or even break, and the connector must be replaced.

2. INTRODUCTION

Helios is an embedded single board computer in the PC/104 small form factor based on the DMP Vortex86DX family of all-in-one 486 processors. Helios integrates a complete embedded PC plus a full analog and digital data acquisition circuit into a single board. It is available in several models with different features:

Model	*Processor Speed*	*Memory*	*Math Coprocessor*	*Digital I/O*	*Analog I/O*
HLV1000-256AV	1GHz	256MB	Yes	40 lines	Yes
HLV1000-256DV	1GHz	256MB	Yes	16 lines	No
HLV800-256AV	800MHz	256MB	Yes	40 lines	Yes
HLV800-256DV	800MHz	256MB	Yes	16 lines	No

The board includes the following key system and data acquisition features:

Processor and Memory

- 1GHz or 800MHz Vortex86DX CPU
- Integrated North Bridge/South Bridge, 10/100 Ethernet MAC/PHY, quad UART, and flash memory with embedded BIOS
- 256MB DDR2 RAM system memory

Video Features

- PCI interface XGI Volari Z9S chip
- Dedicated 32MB video memory
- High performance 2D accelerator
- 18-bit LVDS LCD interface, up to 1600 x 1200
- CRT up to 1600 x 1200

Ethernet

- 10/100Mbps Ethernet circuit integrated into the Vortex processor chip
- On-board transformer and termination network for direct connection to Ethernet cabling

Standard Peripheral Interfaces

- 4 16550-compatible RS-232 ports (2 have RS-422/485 capability)
- 4 USB 2.0 ports
- PS/2 keyboard and mouse ports

  The BIOS supports a USB keyboard during BIOS initialization, and it also supports legacy keyboard emulation via USB for DOS. The USB ports can be used for keyboard and mouse at the same time that the PS/2 keyboard and mouse are connected.

Mass Storage

- 44-pin IDE connector for connection to UDMA-100 hard drive or solid state flashdisk module
- Mounting spacer for rugged mounting of flashdisk in harsh environment applications
- On-board 1.5MB virtual floppy drive in flash memory with FreeDOS pre-installed

Analog I/O

- 16 single-ended or 8 differential analog voltage inputs, 16-bit resolution
- ±1.25V, ±2.5V, ±5V, ±10V, 0-1.25V, 0-2.5V, 0-5V, and 0-10V input ranges
- 250KHz maximum aggregate A/D sampling rate
- Programmable input ranges
- Both bipolar and unipolar input ranges
- Internal and external A/D triggering
- 2048-sample A/D FIFO with programmable threshold
- Auto-calibration of both A/D and D/A circuits
- Four analog voltage outputs, 12-bit resolution
- ±2.5V, ±5V, ±10V 0-5V, and 0-10V output ranges programmable in software

Digital I/O

- Up to 40 programmable digital I/O lines
- Enhanced output current capability: +64mA maximum

Counter/Timers

- One 24-bit counter/timer for A/D sampling rate control
- One 16-bit counter/timer for user counting and timing functions
- Programmable gate and count enable
- Internal (10MHz) or external clock source

Bus Interfaces

The Vortex86DX processor generates both PCI and ISA buses for I/O expansion. The 33MHz 32-bit PCI bus is used internally for the Ethernet circuit and is not brought out to a PCI-104 expansion connector.

The 8MHz 16-bit ISA bus is brought out to a standard PC/104 stackthrough connector, enabling 16-bit and 8-bit modules to be installed either above or below the board. Interrupt and DMA performance is supported on the ISA bus. Up to 4 I/O boards can be installed on the ISA bus on Helios, depending on the loading characteristics of the add-on modules.

Battery Backup

Helios contains a backup battery for the real-time clock and BIOS settings. The battery is directly soldered to the board and provides a minimum 7 year backup lifetime at 25°C. For longer lifetime an external battery of 3.3V +/-10% may be attached to the board.

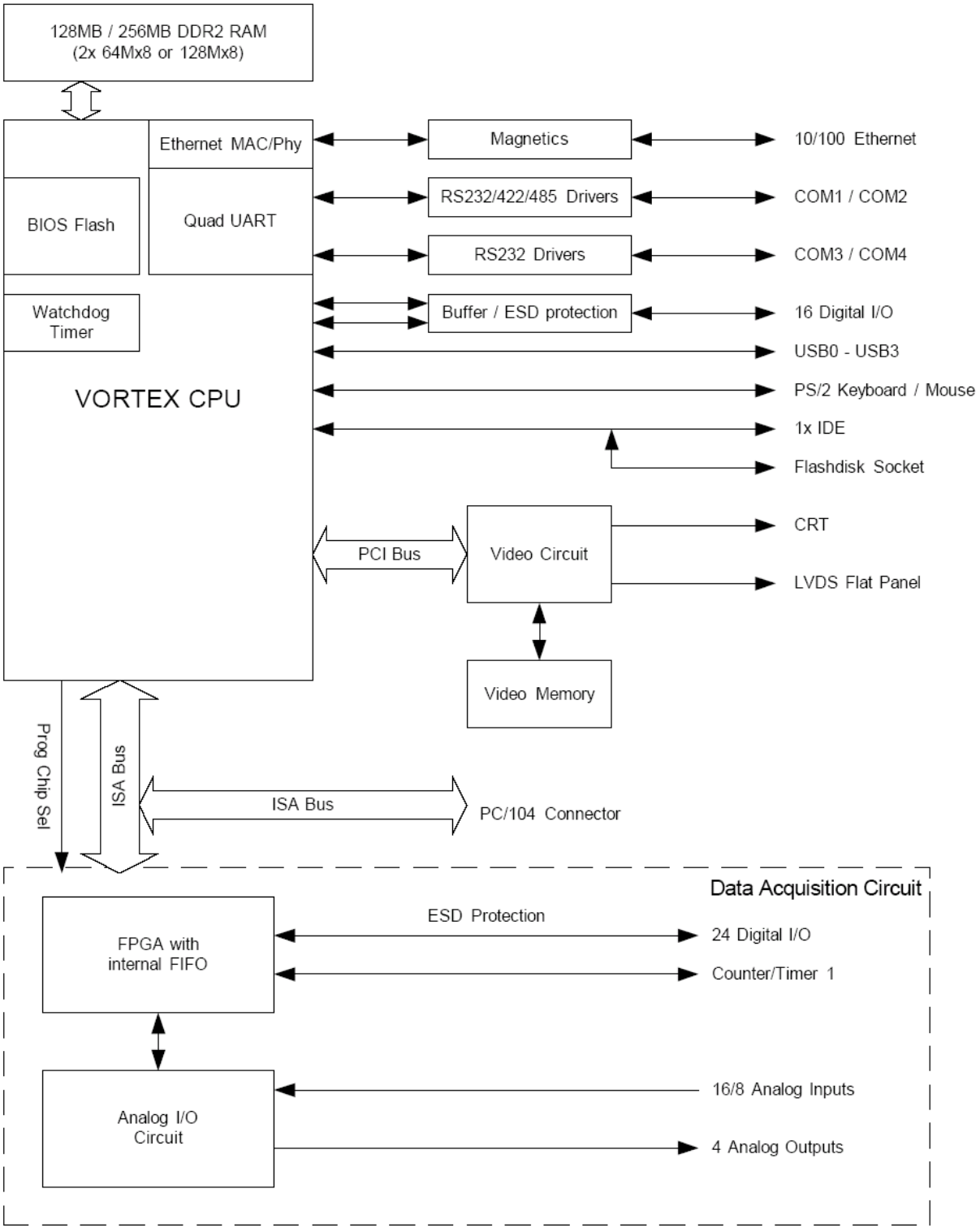
Watchdog Timer

Helios contains a watchdog timer (WDT) circuit with a software-programmable timer. The time delay can be programmed, and the timer can be retriggered with an I/O write command. When the timer times out, it will trigger an IRQ or system reset depending on the user configuration.

Power Supply

Helios requires only +5V +/-5% for operation. The input power connector provides connections for optional provision of +/-12V and -5V for pass through to the ISA bus if needed for attached I/O modules.

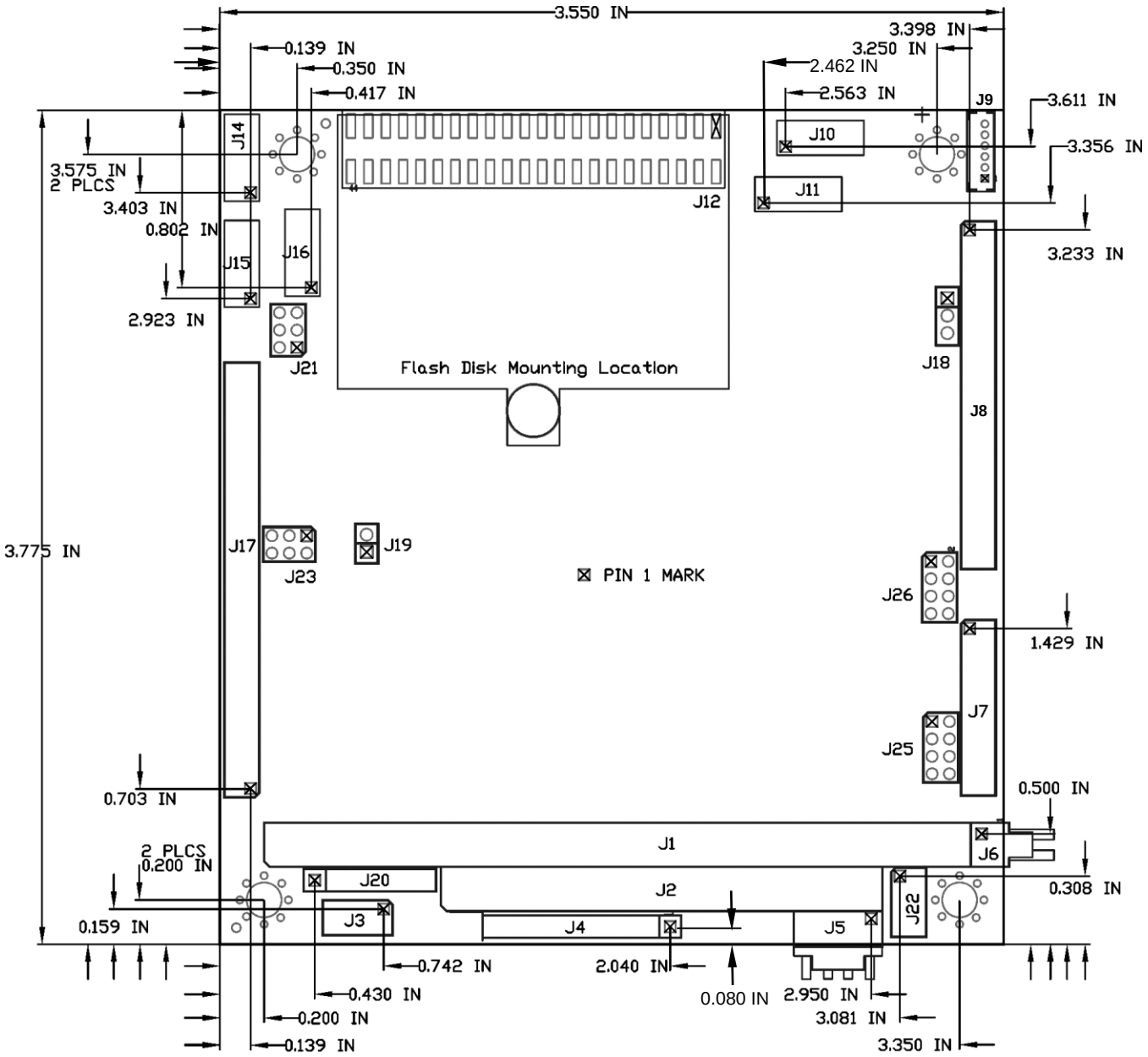
3. FUNCTIONAL BLOCK DIAGRAM



Functional Block Diagram

4. BOARD DIAGRAM

The diagram below shows the board layout, including connectors, jumper blocks and mounting holes.



Helios Board Layout

5. CONNECTOR AND JUMPER LISTS

5.1 I/O Connectors

Connector	*Function*
J1	PC/104, ISA bus 8-bit connector (rows A, B)
J2	PC/104, ISA bus 16-bit connector (rows C, D)
J3	PS/2 keyboard/mouse
J4	Input power
J5	I/O power
J6	External battery
J7	Digital I/O
J8	Serial ports COM1-4
J9	LCD backlight
J10	VGA
J11	Ethernet
J12	IDE
J13	LCD interface (LVDS format) on bottom side
J14	Reset, LEDs
J15	USB 0/1
J16	USB 2/3
J17	Data acquisition I/O
J19	Autocalibration connector (factory use)
J20	Jtag for data acquisition FPGA (factory use)
J22	Panel power input
J24	Jtag for Processor / BIOS flash (factory use)

5.2 Configuration Jumpers

Jumper	*Description*
J18	LCD backlight
J21	DAQ interrupt configuration
J23	Not used
J25	COM1 RS-422/RS-485 configuration
J26	COM2 RS-422/RS-485 configuration

6. I/O CONNECTORS

Note: Pins marked as “key” are cut away or removed.

6.1 Input Power (J4)

Input power may be supplied using either the input power connector J4, the I/O power connector J5, or directly through the PC/104 bus power pins, if a PC/104 power supply is used with the CPU.

The board only requires +5VDC input power to operate. All other required voltages are generated on board. The +12V, -12V, and -5V inputs are provided for convenience and are passed onto the PC/104 bus but are not used by Helios. The +3.3V input is passed through to the LCD connector and may be used to power an attached LCD. Multiple +5V and ground pins are provided for extra current carrying capacity. Each pin is rated at 3A max.

For applications requiring less than 3A, the first four pins may be connected to a standard 4-pin miniature PC power connector, or the alternate power I/O connector may be used. For a larger PC/104 stack the total power requirements should be calculated to determine whether additional power input wires are necessary.

1	+5V In
2	Ground
3	**Key**
4	+12V In
5	Ground
6	+5V In
7	-12V In
8	-5V In
9	+3.3V

Connector type: Standard .1” single row straight pin header with gold flash plating

6.2 I/O Power (J5)

Connector J5 provides an alternate connector for either input power to the system or output power for use with external drives. This connector mates with Diamond Systems cable number 6981006, which provides a standard full-size power connector for a hard drive or CD-ROM drive and a standard miniature power connector for a floppy drive.

1	+5V
2	Ground
3	Ground
4	+12V

Connector type: Standard .1” single row right-angle friction lock pin header

6.3 Panel Power Input (J22)

Connector J22 provides power to the board when connected to the Helios panel I/O board PNL-HLV-02. It is not intended for use as a main power input connector for a power supply cable. All signals are routed to their corresponding pins on the PC/104 bus connectors for use by attached PC/104 modules.

+5V	**1**	**2**	+5V
+5V	**3**	**4**	Ground
Ground	**5**	**6**	Ground
+12V	**7**	**8**	+12V

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.4 Serial Ports (J8)

Connector J8 provides access to the four serial ports of the Vortex CPU. The PORT1 and PORT2 ports are, independently, jumper-configurable for either RS-232, RS-485 or RS-422 protocol. Jumpers J25 and J26 are used to select the protocol. The PORT3 and PORT4 ports are fixed RS-232 protocol. All four serial ports can be independently enabled or disabled in the BIOS.

The following tables list the signal assignments on the pin header for each serial protocol.

In RS-422 and RS-485 modes, the ground on the 5th pin of each port exists only when the "485 GROUND" jumper is installed on jumper configuration blocks J25 and J26. Otherwise these pins are unconnected.

	RS-232 Configuration				RS-422 Configuration				RS-485 configuration			
Port 1	DCD 1	1	2	DSR 1	NC	1	2	NC	NC	1	2	NC
	RXD 1	3	4	RTS 1	TXD+ 1	3	4	TXD- 1	TXD/RXD+ 1	3	4	TXD/RXD- 1
	TXD 1	5	6	CTS 1	GND *	5	6	RXD- 1	GND *	5	6	NC
	DTR 1	7	8	RI 1	RXD+ 1	7	8	NC	NC	7	8	NC
	GND	9	10	NC	GND	9	10	NC	GND	9	10	NC
Port 2	DCD 2	11	12	DSR 2	NC	11	12	NC	NC	11	12	NC
	RXD 2	13	14	RTS 2	TXD+ 2	13	14	TXD- 2	TXD/RXD+ 2	13	14	TXD/RXD- 2
	TXD 2	15	16	CTS 2	GND	15	16	RXD- 2	GND	15	16	NC
	DTR 2	17	18	RI 2	RXD+ 2	17	18	NC	NC	17	18	NC
	GND	19	20	NC	GND	19	20	NC	GND	19	20	NC
Port 3	DCD 3	21	22	DSR 3		21	22			21	22	
	RXD 3	23	24	RTS 3		23	24			23	24	
	TXD 3	25	26	CTS 3		25	26			25	26	
	DTR 3	27	28	RI 3		27	28			27	28	
	GND	29	30	NC		29	30			29	30	
Port 4	DCD 4	31	32	DSR 4		31	32			31	32	
	RXD 4	33	34	RTS 4		33	34			33	34	
	TXD 4	35	36	CTS 4		35	36			35	36	
	DTR 4	37	38	RI 4		37	38			37	38	
	GND	39	40	NC		39	40			39	40	

Connector type: Standard 2mm dual row straight pin header with gold flash plating

Serial ports are typically used with DB9 connectors. The PC / Helios side of the connection uses a male version of the connector and uses the DTE (data terminal equipment) pin assignment. The connecting cable will use a female version of the connector with DCE (data communications equipment) pinout. Diamond's cable number 6981166 provides 4 DB9 connectors with DTE pinout. The following diagram shows the DB-9 male connector pin assignments for each protocol.

In RS-422 and RS-485 modes, the ground on the 3rd pin of each DB9 connector exists only when the "485 GROUND" jumper is installed on jumper configuration blocks J25 and J26. Otherwise these pins are unconnected.

Pin#	RS-232	RS-422	RS-485
1	DCD	NC	NC
2	RXD	TXD+	TXD/RXD+
3	TXD	Ground *	Ground *
4	DTR	RXD+	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	TXD-	TXD/RXD-
8	CTS	RXD-	NC
9	RI	NC	NC

6.5 PS/2 Mouse and Keyboard (J3)

Connector J3 provides the standard PS/2 keyboard and mouse signals.

+5V	1	2	**Key**
KB Data	3	4	MS Data
KB Clk	5	6	MS Clk
Ground	7	8	**Key**

Signal	Definition
+5V	System +5V power
KB Data	Keyboard data
KB Clk	Keyboard clock
MS Data	Mouse data
MS Clk	Mouse clock
Ground	System ground
Key	Key pin (missing on pin header, plugged on mating cable)

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.6 USB (J15, J16)

Helios features four USB 2.0 ports on 2 pin headers. Connector J15 interfaces to USB port 0/1 and connector J16 interfaces to USB ports 2/3. USB 2.0 provides a 480Mbps maximum data transfer rate. The shield pin on each connector is tied to system ground. Diamond Systems' cable number 6981082 mates with these connectors.

J15, USB ports 0 and 1

Key	1	2	Shield
USB1 Pwr-	3	4	USB0 Pwr-
USB1 Data+	5	6	USB0 Data+
USB1 Data-	7	8	USB0 Data-
USB1 Pwr+	9	10	USB0 Pwr+

J16, USB ports 2 and 3

Key	1	2	Shield
USB3 Pwr-	3	4	USB2 Pwr-
USB3 Data+	5	6	USB2 Data+
USB3 Data-	7	8	USB2 Data-
USB3 Pwr+	9	10	USB2 Pwr+

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.7 Ethernet (J11)

The 10/100 Base-T, full-duplex Ethernet interface is provided by connector J11.

TX+	1	2	TX-
NC	3	4	RX-
RX+	5	6	NC
Link LED	7	8	Ground
Key	9	10	100 LED

Signal	Definition
TX+, TX-	Transmit data from CPU
RX+, RX-	Receive data by CPU
Link LED	Indicates valid connection; referenced to ground
100 LED	Indicates 100Mbps data rate established; referenced to ground
Ground	System ground

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.8 VGA (J10)

Connector J10 is used to connect a VGA monitor. Although the DDC serial detection pins are present, a 5V power supply is not provided, and the legacy “Monitor ID” pins are also not used.

RED	1	2	Ground
GREEN	3	4	**Key**
BLUE	5	6	Ground
HSYNC	7	8	DDC-Data
VSYNC	9	10	DDC-Clock

Signal Name	Definition
RED	RED signal (positive, 0.7Vpp into 75 Ohm load)
Ground	Ground return for RED, GREEN, and BLUE signals
GREEN	GREEN signal (positive, 0.7Vpp into 75 Ohm load)
BLUE	BLUE signal (positive, 0.7Vpp into 75 Ohm load)
DDC-CLOCK/DATA	Signals used for monitor detection (DDC1 specification)
Key	Pin missing to match key pin in cable to prevent incorrect connection

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.9 LVDS LCD Interface (J13, bottom side of board)

Connector J13 is used to connect an LVDS LCD. Helios does not support TTL LCDs.

If needed, the LCD backlight can be connected to connector J9.

1	Ground / D3+, depending on video chip
2	Ground / D3-, depending on video chip
3	Scan Direction (High = Reverse Scan, Low/open = Normal Scan)
4	Frame Rate Control (High = On, Low/open = Off)
5	Signal Ground
6	Pixel Clock +
7	Pixel Clock -
8	Signal Ground
9	D2+
10	D2-
11	Signal Ground
12	D1+
13	D1-
14	Signal Ground
15	D0+
16	D0-
17	Power Ground
18	Power Ground
19	Vcc 3.3V / 5V (jumper configured)
20	Vcc 3.3V / 5V (jumper configured)

Connector Part Numbers:

PCB connector:	JAE part no. FI-SE20P-HFE or equivalent
Cable-mount socket:	JAE part no. FI-SE20S-2-L or equivalent

6.10 LCD Backlight (J9)

Connector J9 provides the backlight power and control for an optional LCD panel.

1	LCD Power
2	LCD Power
3	Ground
4	Ground
5	Enable (GPIO output), 0 = off, open circuit = on
6	Brightness, 0-5VDC variable; 0V = max, 5V = min

The LCD power is jumper selectable for +5V or +12V. See the description for J18.

The enable signal controls power to the backlight. It is controlled by digital I/O signal GPIO36.

If 12VDC is needed for the LCD, it must be provided either on one of the input power connectors or on the 12V pin (J1, B9) of the PC/104 connector. The board does not generate 12V internally.

The brightness control for the LCD backlight has a weak pull-down resistor to ensure maximum brightness when it is not connected externally.

Connector Part Numbers:

Connector on CPU board:	Molex 53047-0610 or equivalent
Mating cable connector:	Socket: Molex 51021-0600 or equivalent
Terminals for mating connector:	Molex 50058 / 50079 series or equivalent

6.11 IDE (J12)

The IDE connector is a standard notebook hard drive type 2x22 (44-pin) 2mm-pitch pin header. It mates with Diamond Systems' cable number 6981004, and may be used to connect up to 2 IDE drives (hard disks, CD-ROMs, or flashdisk modules). An IDE flashdisk may also be installed on this connector to provide rugged, wide temperature solid state storage up to 4GB. Pin 20 is removed for keying to prevent incorrect cable installation.

RESET-	**1**	**2**	Ground
D7	**3**	**4**	D8
D6	**5**	**6**	D9
D5	**7**	**8**	D10
D4	**9**	**10**	D11
D3	**11**	**12**	D12
D2	**13**	**14**	D13
D1	**15**	**16**	D14
D0	**17**	**18**	D15
Ground	**19**	**20**	**Key**
DRQ	**21**	**22**	Ground
IDEIOW-	**23**	**24**	Ground
IDEIOR-	**25**	**26**	Ground
IORDY	**27**	**28**	Ground
DACK-	**29**	**30**	Ground
IRQ14	**31**	**32**	Pulled low for 16-bit operation
A1	**33**	**34**	Not Used
A0	**35**	**36**	A2
CS0-	**37**	**38**	CS1-
LED-	**39**	**40**	Ground
+5V	**41**	**42**	+5V
Ground	**43**	**44**	Not Used

Connector type: Standard 2mm dual row SMT straight pin header with gold flash plating

6.12 External Battery (J6)

Connector J6 is used to connect an optional external battery to replace the on-board backup battery. The on-board battery provides about 7 years of lifetime at an ambient temperature of 25^{o}C. For longer lifetime an external battery of 3.3V ±10% may be connected to this connector.

1	Ground
2	Battery+

Connector type: Standard .1" single row right-angle friction lock pin header

6.13 Digital I/O (J7)

Connector J7 provides 16 digital I/O lines from the Vortex CPU. These lines are buffered and have ESD protection to protect the CPU from potential damage. The buffers enable the direction to be programmed in 8-bit groups, using two additional GPIO lines from the Vortex processor. The direction may be set in the BIOS or by programming the CPU I/O control registers.

DIO D0	**1**	**2**	DIO D1
DIO D2	**3**	**4**	DIO D3
DIO D4	**5**	**6**	DIO D5
DIO D6	**7**	**8**	DIO D7
DIO E0	**9**	**10**	DIO E1
DIO E2	**11**	**12**	DIO E3
DIO E4	**13**	**14**	DIO E5
DIO E6	**15**	**16**	DIO E7
+5V	**17**	**18**	Ground
Key	**19**	**20**	Ground

Signal	Definition
DIO D7-0	GPIO port 0 from Vortex CPU
DIO E7-0	GPIO port 1 from Vortex CPU
+5V	Connected to main +5V supply
Ground	Digital ground

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.14 Data Acquisition (J17)

Connector J17 is provided for the AV model with data acquisition. Diamond Systems cable number 6981163 provides a 50-pin connector with both 2mm and .1" pitch connectors for use with this connector.

DIO A0	1	2	DIO A1
DIO A2	3	4	DIO A3
DIO A4	5	6	DIO A5
DIO A6	7	8	DIO A7
DIO B0	9	10	DIO B1
DIO B2	11	12	DIO B3
DIO B4	13	14	DIO B5
DIO B6	15	16	DIO B7
DIO C0	17	18	DIO C1
DIO C2	19	20	DIO C3
DIO C4 / Gate 0	21	22	DIO C5 / Gate 1
DIO C6 / Clk 1	23	24	DIO C7 / Out 0
Ext Trig	25	26	Out 1
+5V Out	27	28	Dground
Vout 0	29	30	Vout 1
Vout 2	31	32	Vout 3
Aground (Vout)	33	34	Aground (Vin)
Vin 0	35	36	Vin 8
Vin 1	37	38	Vin 9
Vin 2	39	40	Vin 10
Vin 3	41	42	Vin 11
Vin 4	43	44	Vin 12
Vin 5	45	46	Vin 13
Vin 6	47	48	Vin 14
Vin 7	49	50	Vin 15

Signal Name	Definition
DIO A7-A0	Digital I/O port A; programmable direction
DIO B7-B0	Digital I/O port B; programmable direction
DIO C7-C0	Digital I/O port C; programmable direction
	C7-C4 may be configured for counter/timer signals
Ext Trig	External A/D trigger input
Out 1	Counter/Timer 1 output
Vin 7/7+ ~ Vin 0/0+	Analog input channels 7 – 0 in single-ended mode;
	High side of input channels 7 – 0 in differential mode
Vin 15/7- ~ Vin 8/0-	Analog input channels 15 – 8 in both single-ended mode;
	Low side of input channels 7 – 0 in differential mode
Vout0-3	Analog output channels 0 – 3
+5V Out	Connected to switched +5V supply
Aground (Vout), (Vin)	Analog ground; used for analog circuitry only
	Vout pin is for the analog outputs; Vin pin is for the analog inputs
Dground	Digital ground; used for digital circuitry only

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.15 Miscellaneous (J14)

Connector J14 provides access to common miscellaneous signals used in a PC application.

Ground	1	2	Reset-
IDE LED	3	4	+5V
Key	5	6	Power LED
Reserved	7	8	LCD Backlight Ctrl
Speaker	9	10	+5V

Signal	Definition
Speaker	The signal on this pin is referenced to +5V Out. Connect a speaker between this pin and +5V Out.
IDE Drive LED	Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out.
Power LED	Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out.
Reset-	Connection between this pin and Ground will generate a Reset condition.
LCD Backlight Ctrl	User provided brightness control for the LCD backlight; 0V = max, 5V = min. This signal has a pull-down resistor to ensure maximum brightness when it is not connected externally.
Reserved	Not connected, reserved for future use.

Connector type: Standard 2mm dual row straight pin header with gold flash plating

6.16 Autocalibration (J19)

Connector J19 is used on the Helios AV model for factory calibration of the analog I/O circuit. A precision voltmeter is connected to this connector to measure the on-board references during the calibration process.

1	Ground
2	VCAL

Connector type: Standard .1” single row straight pin header with gold flash plating

6.17 FPGA Programming (J20)

Connector J20 is the JTAG configuration interface for factory use and firmware upgrade of the FPGA in the data acquisition circuit on the Helios AV model.

1	+5V
2	Ground
3	TCK
4	TDO
5	TDI
6	TMS

Connector type: Standard .1” single row straight pin header with gold flash plating

6.18 PC/104 ISA Bus (J1, J2)

The PC/104 bus is essentially identical to the ISA Bus except for the physical design. It specifies two pin and socket connectors for the bus signals. A 64-pin header J1 incorporates the 62-pin 8-bit bus connector signals, and a 40-pin header J2 incorporates the 36-pin 16-bit bus connector signals. The additional pins on the PC/104 connectors are used as ground or key pins. The female sockets on the top of the board enable stacking another PC/104 board on top of the board, while the male pins on the bottom enable the board to plug into another board below it.

In the pinout figures below, the tops correspond to the left edge of the connector when the board is viewed from the primary side (side with the CPU chip and the female end of the PC/104 connector) and the board is oriented so that the PC/104 connectors are along the bottom edge of the board.

View from Top of Board

J2: PC/104 16-bit bus connector

Ground	**D0**	**C0**	Ground
MEMCS16-	**D1**	**C1**	SBHE-
IOCS16-	**D2**	**C2**	LA23
IRQ10	**D3**	**C3**	LA22
IRQ11	**D4**	**C4**	LA21
IRQ12	**D5**	**C5**	LA20
IRQ15	**D6**	**C6**	LA19
IRQ14	**D7**	**C7**	LA18
DACK0-	**D8**	**C8**	LA17
DRQ0	**D9**	**C9**	MEMR-
DACK5-	**D10**	**C10**	MEMW-
DRQ5	**D11**	**C11**	SD8
DACK6-	**D12**	**C12**	SD9
DRQ6	**D13**	**C13**	SD10
DACK7-	**D14**	**C14**	SD11
DRQ7	**D15**	**C15**	SD12
+5V	**D16**	**C16**	SD13
MASTER-	**D17**	**C17**	SD14
Ground	**D18**	**C18**	SD15
Ground	**D19**	**C19**	Key (pin cut)

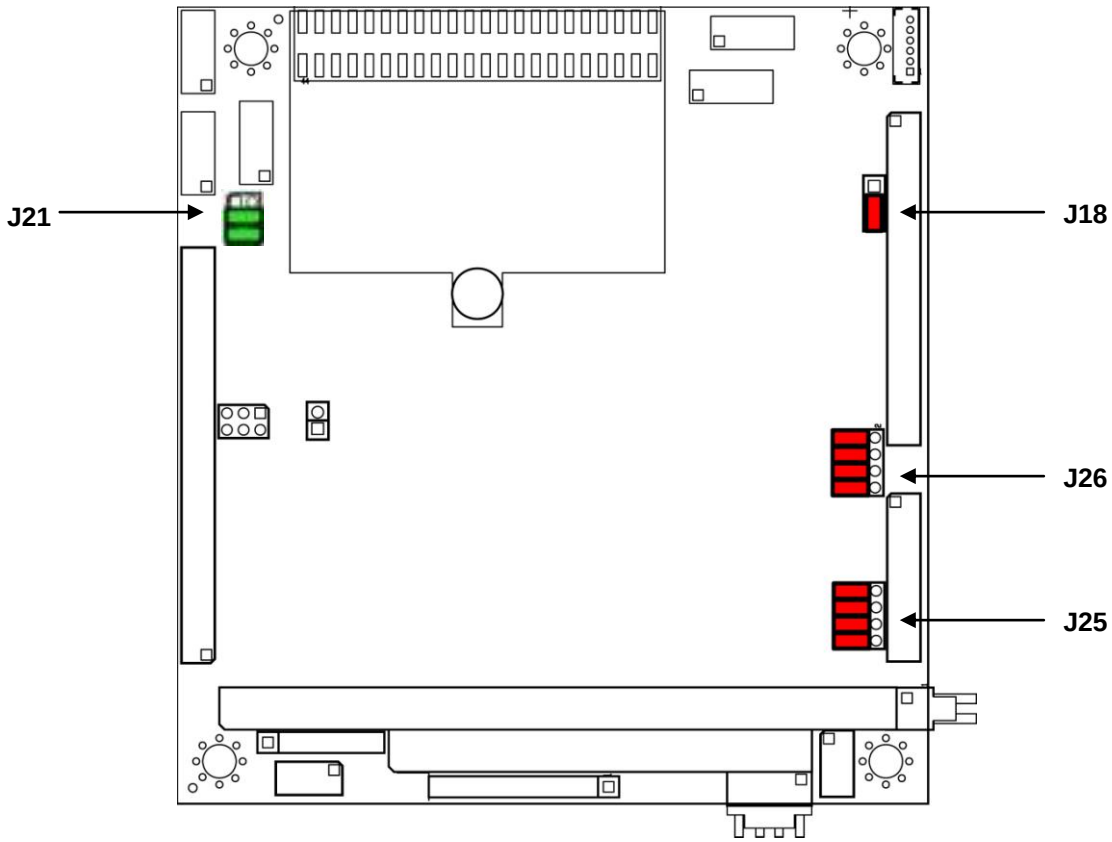
J1: PC/104 8-bit bus connector

IOCHCHK-	**A1**	**B1**	Ground
SD7	**A2**	**B2**	RESET
SD6	**A3**	**B3**	+5V
SD5	**A4**	**B4**	IRQ9
SD4	**A5**	**B5**	-5V
SD3	**A6**	**B6**	DRQ2
SD2	**A7**	**B7**	-12V
SD1	**A8**	**B8**	0WS-
SD0	**A9**	**B9**	+12V
IOCHRDY	**A10**	**B10**	Key (pin cut)
AEN	**A11**	**B11**	SMEMW-
SA19	**A12**	**B12**	SMEMR-
SA18	**A13**	**B13**	IOW-
SA17	**A14**	**B14**	IOR-
SA16	**A15**	**B15**	DACK3-
SA15	**A16**	**B16**	DRQ3
SA14	**A17**	**B17**	DACK1-
SA13	**A18**	**B18**	DRQ1
SA12	**A19**	**B19**	Refresh-
SA11	**A20**	**B20**	SYSCLK
SA10	**A21**	**B21**	IRQ7
SA9	**A22**	**B22**	IRQ6
SA8	**A23**	**B23**	IRQ5
SA7	**A24**	**B24**	IRQ4
SA6	**A25**	**B25**	IRQ3
SA5	**A26**	**B26**	DACK2-
SA4	**A27**	**B27**	TC
SA3	**A28**	**B28**	BALE
SA2	**A29**	**B29**	+5V
SA1	**A30**	**B30**	OSC
SA0	**A31**	**B31**	Ground
Ground	**A32**	**B32**	Ground

7. CONFIGURATION JUMPERS

Helios contains the following configuration jumper blocks. The diagram below shows the default jumper settings.

Jumper	*Description*
J18	LCD backlight
J21	DAQ interrupt configuration
J25	COM1 RS-422/RS-485 configuration
J26	COM2 RS-422/RS-485 configuration



7.1 LCD Backlight Power (J18)

Jumper block J18 configures the voltage supply for the LCD backlight. Although the diagrams below show labels on the jumper block, there are no labels on the board. The orientation of the block in the diagrams matches the orientation of the jumper block when the board is rotated so that the PC/104 connector is on the lower edge (facing you).

Available options are +5V from the main power supply input or +12V from the auxiliary +12V input. +12V is not used by any circuit on the Helios CPU, so it is not required to provide it on the input power connector. If +12V is needed for the LCD backlight, and the backlight is to be powered via the backlight power connector J9, then +12V must be supplied on the main power input connector along with +5V.

+5V power **+12V power**

7.2 Data Acquisition Interrupt Configuration (J21)

Jumper block J21 is used to configure the data acquisition circuit interrupt selection and interrupt pull-down resistor on the AV model of Helios. Although the diagrams below show labels on the jumper block, there are no labels on the board. The orientation of the block in the diagrams matches the orientation of the jumper block when the board is rotated so that the PC/104 connector is on the lower edge (facing you).

If you will use interrupt-based A/D sampling, select one of the available IRQs, 5 or 6, by installing a jumper in the two pins underneath the desired IRQ level. Select only one IRQ level. The IRQ must also be configured in the BIOS as "Reserved" to make it available to the PC/104 bus. The default setting is IRQ5, and the default BIOS configuration reserves IRQ5 for the PC/104 bus.

On the PC/104 bus, interrupt signals are driven high when active and tri-stated when inactive. To drive the inactive line to a valid logic level, a 1KΩ pull-down resistor must be attached to any IRQ that is being used. Since the line is only driven high and never low, this technique allows multiple boards to share the same IRQ, because there is never a conflict from two boards driving the IRQ in opposing logic levels. To make shared interrupts work, the interrupt service routine must check the board's status register to determine whether the board generated the interrupt, and must be able to pass control to another interrupt routine for the same level if needed.

If multiple boards are sharing the same IRQ, only one of them can have the pull-down resistor connected in order to ensure proper loading of the signal. Therefore the pull-down resistor is provided as a jumper-configurable option. If Helios is the only board using the assigned IRQ, then install the jumper for the pull-down resistor. If more than one board is using the same IRQ, then one board should have the pull-down resistor connected, and the other boards should each have their pull-down resistor unconnected. The default setting is jumper installed for pull-down resistor connected.

J21 Jumper configurations

IRQ5 with pulldown **IRQ5 no pulldown** **IRQ6 with pulldown** **IRQ6 no pulldown**

Label	*Function*
IRQ6	Selects IRQ6 for the data acquisition circuit
IRQ5	Selects IRQ5 for the data acquisition circuit
PULLDOWN	Enables 1KΩ pull-down resistor for the data acquisition IRQ selected

7.3 RS-422/RS-485 Configuration (J25, J26)

Use J25 to select the COM1 RS-422/RS-485 termination and J26 to select the COM2 RS-422/RS-485 termination. Any port configured for RS-232 should not have any jumpers installed. COM3 and COM4 are fixed RS-232, so no termination configuration is available for them.

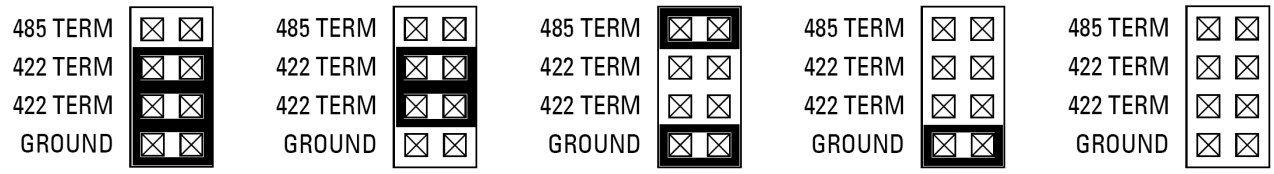
Although the diagrams below show labels on the jumper blocks, there are no labels on the board. The orientation of the block in the diagrams matches the orientation of the jumper block when the board is rotated so that the PC/104 connector is on the lower edge (facing you).

For RS-422: Installing two jumpers in the 422 TERM positions as shown will connect a 120 ohm termination resistor across the RX + and – lines and will also connect 1K ohm bias resistors to the RX lines. The + line is biased toward ground, and the – line is biased toward +5V. This sets the receiver to an inactive state when the receiver is unconnected. Both jumpers should be installed if termination / biasing is desired. Installing only one jumper will create unpredictable behavior by the receiver.

For RS-485: Installing a jumper in the 485 TERM position will connect a 120 ohm resistor across the differential driver/receiver pair. The RS-485 network should have a termination resistor installed at each end of the circuit but not at intermediate nodes.

For both RS-422 and RS-485: Installing a jumper in the GROUND position will provide a second signal ground on the 5th pin of each serial port's 10-pin group on the serial port connector J8. This corresponds to pin 3 of a DB9 male connector when Diamond's cable 6981166 is attached to connector J8. Each port already has a ground on pin 9 of the 10-pin group, corresponding to pin 5 on a DB9 male connector.

J25/J26 Jumper Configurations



RS-422 bias + gnd | **RS-422 bias only** | **RS-485 term + gnd** | **RS-485 gnd only** | **RS-232**

Label	*Function*
485 TERM	RS-485 Tx termination resistor
422 TERM	RS-422 Rx termination and bias resistors
GROUND	2nd ground pin for RS-422 / RS-485

8. SYSTEM RESOURCES

The table below lists the default system resources utilized by the circuits on Helios.

Device	*I/O Address*	*ISA IRQ*	*ISA DMA*
Serial Port COM1	0x3F8 – 0x3FF	4	–
Serial Port COM2	0x2F8 – 0x2FF	3	–
Serial Port COM3	0x3E8 – 0x3EF	10	–
Serial Port COM4	0x2E8 – 0x2EF	11	–
IDE Controller	0x1F0 – 0x1F7	14	–
A/D Circuit (when installed)	0x280 – 0x28F	5	–
Serial Port/FPGA Control	0x25C – 0x25F	–	–
Watchdog Timer	0x67 – 0x6D	–	–
Ethernet	OS-dependent	OS-dependent	–
USB	OS-dependent	OS-dependent	–
Sound	OS-dependent	OS-dependent	–
Video	OS-dependent	OS-dependent	–
Vortex CPU digital I/O	0x78 – 0x7C 0x98 – 0x9C	–	–

Most of these resources are configurable and, in many cases, the operating system alters these settings. The main devices that are subject to this dynamic configuration are on-board Ethernet, sound, video, USB, and any PC/104-*Plus* cards that are in the system. These settings may also vary depending on what other devices are present in the system. For example, adding a PC/104-*Plus* card may change the on-board Ethernet resources. The serial port settings for COM1 and COM2 are jumper-selectable (J25, J26), whereas the settings for COM3 and COM4 are entirely software-configured in the BIOS.

9. VIDEO FEATURES

Helios includes a video subsystem that provides both CRT and LCD output with several choices of resolution. The resolution is fixed in the BIOS but can be changed with a software utility provided on the Diamond Systems CD.

LCD Resolution	*CRT Auto-Adapt*	*Note*
320 x 240		
640 x 480	Yes	Default resolution
800 x 480		
800 x 600	Yes	
1024 x 600		
1024 x 768	Yes	

9.1 CRT

Helios provides a standard CRT port on connector J10. The resolution of the CRT output matches the resolution configured in the BIOS for the LCD. An attached monitor should be able to automatically adapt for many of the available resolutions. If the monitor does not adapt properly, either adjust the monitor settings, change the LCD/CRT resolution in the BIOS (see separate instructions), or use a different monitor.

Note: The BIOS setup screens and DOS display are always configured for 640x480 resolution, regardless of the display resolution selected in the BIOS. If you configure the BIOS for a different resolution, the display may not look correct when you are in the BIOS setup screens or in DOS. For example, if the screen is set for 1024x768, the BIOS and DOS screens will appear smaller than full screen and will generally be centered in the screen with a blank border around them. If you are using DOS, the optimum CRT resolution is 640x480. This same advice may apply for a text-based Linux environment as well.

Diamond Systems cable number 6981178 is used to connect a monitor to connector J10. It provides a standard DB15 female connector for a CRT.

CRT connector J10

RED	**1**	**2**	Ground
GREEN	**3**	**4**	**Key**
BLUE	**5**	**6**	Ground
HSYNC	**7**	**8**	DDC-Data
VSYNC	**9**	**10**	DDC-Clock

Signal Name	Definition
RED	RED signal (positive, 0.7Vpp into 75 Ohm load)
Ground	Ground return for RED, GREEN, and BLUE signals
GREEN	GREEN signal (positive, 0.7Vpp into 75 Ohm load)
BLUE	BLUE signal (positive, 0.7Vpp into 75 Ohm load)
DDC-CLOCK/DATA	Signals used for monitor detection (DDC1 specification)
Key	Pin missing to match key pin in cable to prevent incorrect connection

9.2 LCD

There are two common types of LCD signaling used in embedded computers: LVDS and TTL. The LCD output on Helios uses the more popular LVDS (low-voltage differential signaling) format. If you are planning to use a TTL LCD with Helios, you will need to use a small adapter board that converts LVDS to TTL. Many such boards are available from suppliers.

The LCD used with Helios must match the programmed resolution and scan rate in the Helios BIOS. These settings can be changed with a software utility provided with the board (see below). Helios provides 18-bit LVDS output, so the LCD selected must work with 18-bit data.

As opposed to CRTs, there is no standard LCD connector type or format. Each LCD manufacturer has its own standards, and there are also different specifications such as the number of data bits used in the video signal. You will need to create your own LCD cable to connect from the LCD connector on Helios to the input connector on your LCD. For assistance with signal definitions or wiring requirements, contact the LCD maker or Diamond technical support. Diamond offers cable no. 6981206 with the correct connector type and pinout to match the LCD connector on Helios. The other end may need to be changed to work with your LCD.

Connector J13 is used to connect an LVDS LCD to Helios:

1	Ground / D3+, depending on video chip
2	Ground / D3-, depending on video chip
3	Scan Direction (High = Reverse Scan, Low/open = Normal Scan)
4	Frame Rate Control (High = On, Low/open = Off)
5	Signal Ground
6	Pixel Clock +
7	Pixel Clock -
8	Signal Ground
9	D2+
10	D2-
11	Signal Ground
12	D1+
13	D1-
14	Signal Ground
15	D0+
16	D0-
17	Power Ground
18	Power Ground
19	Vcc 3.3V / 5V (jumper configured)
20	Vcc 3.3V / 5V (jumper configured)

If needed, the LCD backlight can be connected to connector J9:

1	Backlight Power
2	Backlight Power
3	Ground
4	Ground
5	Enable (GPIO output), 0 = off, open circuit = on
6	Brightness, 0-5VDC variable; 0V = max, 5V = min

The backlight power is jumper-selectable between +5V and +12V using jumper block J18. If 12VDC is needed for the LCD, it must be provided either on one of the input power connectors or on the 12V pin (J1, B9) of the PC/104 connector. The board does not generate 12V internally.

WARNING: Be sure the proper voltage is configured BEFORE connecting the cable to your backlight inverter, or it could be damaged.

The brightness control for the LCD backlight has a weak pull-down resistor to ensure maximum brightness when it is not connected externally.

Diamond offers cable number 6981207 with the correct connector type and pinout to match the backlight power connector on Helios. The other end may need to be changed to work with your LCD backlight inverter.

The enable signal on J9 controls power to the backlight. It is controlled by Helios GPIO signal Port 3 Bit 6. The LCD display can also be enabled or disabled by using GPIO signal Port 3 Bit 5. To control these settings in software, do the following:

1. Set GPIO direction control register to output:

```
outp(0x9B, 3);                // sets bits 1 and 0 of GPIO port 3 to output
```

2. Set bit 5 of port 3 to 1 to enable or 0 to disable the LCD display. Default setting is enabled.

```
outp(0x7B, inp(0x7B) | 0x20); // Port 3 bit 5 = 1 for LCD enable
outp(0x7B, inp(0x7B) & 0xDF); // Port 3 bit 5 = 0 for LCD disable
```

3. Set bit 6 of port 3 to 1 to enable or 0 to disable the backlight. Default setting is enabled.

```
outp(0x7B, inp(0x7B) | 0x40); // Port 3 bit 6 = 1 for backlight enable
outp(0x7B, inp(0x7B) & 0xBF); // Port 3 bit 6 = 0 for backlight disable
```

The LCD backlight can also be configured in the BIOS. Select **Chipset**, then **South Bridge Configuration** menu. The backlight can be enabled or disabled, and its brightness can be set to min or max.

9.3 Changing the LCD / CRT Resolution

The LCD / CRT resolution on Helios is controlled by an "extension" embedded in the BIOS. The extension provides only a single fixed resolution. The extension can be swapped with another one to change the resolution using the instructions below.

The available LCD resolutions are shown below. Diamond provides preconfigured BIOS images for each available resolution. The default BIOS loaded on boards delivered by Diamond is 1024x768. In the filenames shown, the letter "A" indicates the revision of the file and may be different. If more than one revision is available, select the highest letter or the one that matches your needs.

LCD Resolution	*Preconfigured BIOS*	*CRT Auto-Adapt*	*Note*
320 x 240	HLV3224A.ROM		
640 x 480	HLV6448A.ROM	Yes	Default BIOS Image
800 x 480	HLV8048A.ROM		
800 x 600	HLV8060A.ROM	Yes	
1024 x 600	HLV1060A.ROM		
1024 x 768	HLV1076A.ROM	Yes	

There are two methods of updating the LCD resolution:

- If you are using the standard BIOS, then you can simply use one of the preconfigured BIOS images for Helios that already contains the desired resolution. Refer to section 9.3.2. You will need to change any custom settings after updating the BIOS.

- If you have a BIOS with custom default settings, then you need to modify your existing BIOS image by replacing the LCD BIOS extension with a new one. Refer to section 9.3.1.

9.3.1 Modifying the BIOS with a New LCD Resolution

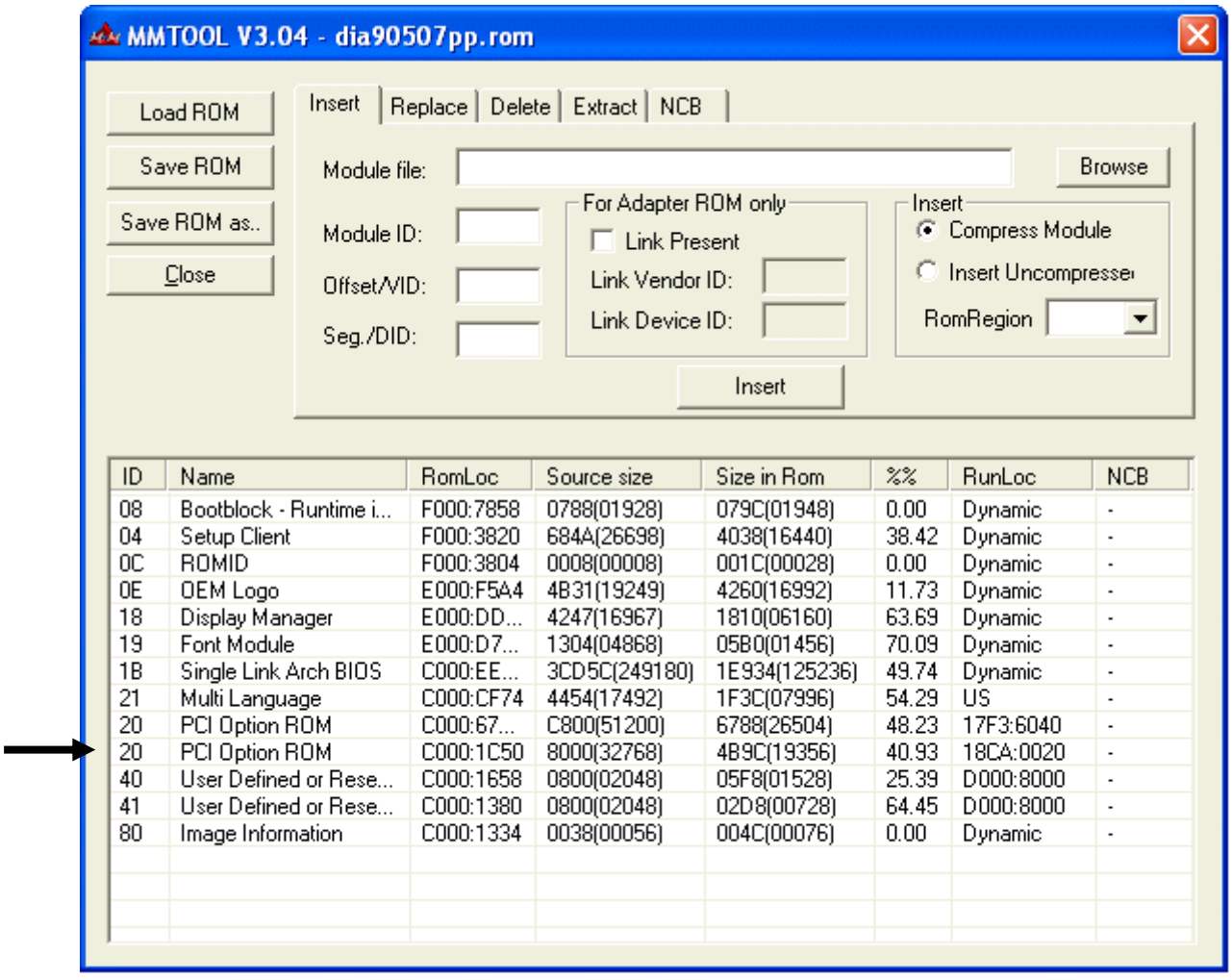
The BIOS image is modified by using a Windows XP utility called MMTOOL.EXE that can be run on any Windows XP computer.

You will need the following items to modify the BIOS image:

1. PC with Windows XP
2. MMTOOL software
3. Existing Helios BIOS image
4. Helios LCD BIOS extension files
5. Bootable device with DOS or FREEDOS, such as an IDE flashdisk or USB memory stick
6. SPIFLASH software

Instructions for MMTOOL software:

1. Start the MMTOOL software on the Windows computer.
2. Click on the "Load ROM" button.
3. Select the desired BIOS image file from the table above and click on the **"Open"** button. The following screen will appear:



ID	Name	RomLoc	Source size	Size in Rom	%%	RunLoc	NCB
08	Bootblock - Runtime i...	F000:7858	0788(01928)	079C(01948)	0.00	Dynamic	-
04	Setup Client	F000:3820	684A(26698)	4038(16440)	38.42	Dynamic	-
0C	ROMID	F000:3804	0008(00008)	001C(00028)	0.00	Dynamic	-
0E	OEM Logo	E000:F5A4	4B31(19249)	4260(16992)	11.73	Dynamic	-
18	Display Manager	E000:DD...	4247(16967)	1810(06160)	63.69	Dynamic	-
19	Font Module	E000:D7...	1304(04868)	05B0(01456)	70.09	Dynamic	-
1B	Single Link Arch BIOS	C000:EE...	3CD5C(249180)	1E934(125236)	49.74	Dynamic	-
21	Multi Language	C000:CF74	4454(17492)	1F3C(07996)	54.29	US	-
20	PCI Option ROM	C000:67...	C800(51200)	6788(26504)	48.23	17F3:6040	-
20	PCI Option ROM	C000:1C50	8000(32768)	4B9C(19356)	40.93	18CA:0020	-
40	User Defined or Rese...	C000:1658	0800(02048)	05F8(01528)	25.39	D000:8000	-
41	User Defined or Rese...	C000:1380	0800(02048)	02D8(00728)	64.45	D000:8000	-
80	Image Information	C000:1334	0038(00056)	004C(00076)	0.00	Dynamic	-

4. Click on the item indicated by the arrow. Make sure the ID, Name, and RunLoc values match what is shown.

5. Click on the **"Replace"** tab.
6. Click on the "Browse" button and select the BIOS extension file that has the desired LCD resolution, then click "Open" to accept the file and close the dialog box. The BIOS extension files are listed below. Note that the BIOS extension files have an extension of .bin instead of .rom. In the filenames shown, the letter "A" indicates the revision of the file and may be different for the actual files.

LCD Resolution	*BIOS Extension File*
320 x 240	HLV-LCD3224A.BIN
640 x 480	HLV-LCD6448A.BIN
800 x 480	HLV-LCD8048A.BIN
800 x 600	HLV-LCD8060A.BIN
1024 x 600	HLV-LCD1060A.BIN
1024 x 768	HLV-LCD1076A.BIN

7. Click on **"Replace"** to replace the item in the list with the new BIOS extension. The screen will display the updated information.
8. If you get an error message "Error – ROM space isn't enough", then you have selected an invalid file. Check your selection again or contact Diamond technical support for assistance.
9. Click on **"Save ROM as.."**, type in the new filename, and click on OK.

   The filename must conform to the DOS 8-character naming convention.

9.3.2 Updating the BIOS with SPIFLASH Software

The BIOS image is programmed into the Helios SBC by using the SPIFLASH utility program.

1. Create a DOS bootable mass storage device such as an IDE flashdisk or a USB memory stick.
2. Copy the desired BIOS image file and the SPIFLASH utility program to the boot device.
3. Install the boot device on the Helios board and power it up.
4. At the DOS prompt, type the following command. <filename.rom> is the name of the BIOS image file. The filename must conform to the DOS 8-character naming convention.

```
spiflash u <filename.rom>
```

5. SPIFLASH will automatically reprogram the Helios SBC's BIOS image and provide a progress indicator. The program will indicate successful completion of the process, which should take about 10 seconds.
6. Restart the system and press the **DEL** key to enter the BIOS SETUP utility.
7. Hit the left arrow key once to go to the tab labeled "Exit." Select "Load optimal defaults" using the up/down arrow keys, and hit **Enter** to confirm. Then select "Save and Exit," and hit **Enter** to confirm.
8. This completes the BIOS process. Reboot the system with the LCD attached to verify proper performance.

10. INSTALLATION AND CONFIGURATION

This section describes the steps needed to get your Helios SBC up and running, and assumes that you also have a Helios Development Kit or Helios Cable Kit. The Cable Kit includes all cables needed for the I/O, except the LCD and backlight. The Development Kit includes the Cable Kit, an AC adapter to power the board, an IDE flashdisk, and the flashdisk programmer board.

10.1 Quick Setup

1. Attach VGA cable 6981084, PS/2 keyboard / mouse cable 6981083, and USB cables 6981082 as needed.
2. Attach display, keyboard, and mouse (if needed) to the cables.
3. Connect power to power input connector J4 using AC adapter PS-5V-04 or your own power supply with power cable 6981009. The input connector and cable keyed to prevent incorrect connection. However ensure that the red wire +5V is on pin 1 of the board connector J4.

   WARNING: Attaching the power connector incorrectly will destroy the Helios SBC!
4. For a quick verification that the system is set up and working properly, if no boot device is attached, the system will boot to FreeDOS on the on-board virtual flash drive. In order for this to work, the on-board flash drive must be enabled. See instructions in section 11.4.

10.2 Boot Device Options

Helios can boot to an IDE device, a USB device, or the on-board 2MB virtual floppy drive. Helios has a single IDE channel that can support up to two devices simultaneously (Master and Slave). IDE devices connect to J12, which is a 44-pin, laptop style IDE connector. This connector has pin 20 cut to match the key pin on Diamond cable number 6981004.

WARNING: It is possible to destroy the Helios SBC by connecting an IDE cable incorrectly (reverse orientation or offset from correct position). Always used keyed cables to avoid connection errors.

The Boot device selection and priority are configured in the BIOS **Boot** menu. See Chapter 11 for detailed BIOS instructions. Only devices which are currently attached to the SBC will appear in the list of options. Therefore if you want to select a hard drive or USB device as the boot device, you must connect it to the SBC first, then boot up and enter the BIOS, then select it as a boot device.

The following are a few example boot scenarios.

- Install an IDE flashdisk directly on the IDE connector J12.
- Connect a laptop IDE hard drive directly to J12 through a 44-pin ribbon cable such as Diamond Systems cable 6981004.
- Use cable 6981004 to connect an IDE flashdisk programmer board to J12. You can then install a flashdisk on the programmer board and connect another 40-pin or 44-pin IDE compatible device to the programmer board. Note that the 44-pin cable will provide +5V power from the SBC to the IDE device, but the 40 pin cable does not carry +5V, so you will need to provide power separately. You can use cable 6981006, attached to J5 on Helios, to provide power from the board to 40-pin devices.
- Attach a bootable USB device to one of the USB ports with USB cable number 6981082.
- Attach no external storage device to Helios. The system will boot to the FreeDOS installed on the on-board virtual floppy drive, as long as it is enabled in the BIOS.

11. BIOS FUNCTIONS

The BIOS on Helios provides access to many valuable features. These instructions show how to enter the BIOS, set up features, and restore the BIOS to its default settings.

11.1 Entering the BIOS

The BIOS may be entered during startup by pressing the **DEL** key on an attached keyboard or pressing **F4** if using console redirection. Press the key repeatedly right after power-on or reset until the BIOS screen appears.

After a certain amount of time during startup, the BIOS will ignore the DEL or F4 key. If you wait too long and the system does not respond, simply reset the board (or power down) and try again.

BIOS setup screens are in 640x480 resolution regardless of the screen resolution programmed in the BIOS. For optimum use of the BIOS setup screens, be sure to select a resolution of 640x480 or higher. After you are finished with BIOS configuration, you can update the BIOS with a lower resolution if desired.

11.2 Restoring Default BIOS Settings

When you make changes to the BIOS settings, the new settings are stored in a battery-backed CMOS RAM built into the Vortex processor. If you want to restore the BIOS settings to their defaults, you can do that by erasing the CMOS RAM using the following procedure.

1. Connect a keyboard to the PS/2 keyboard port and connect a monitor. Erasing CMOS RAM is not available with console redirection.
2. Reboot the CPU (reset or power-down and power-up).
3. Hold down the **END** key while the CPU is booting.
4. The board will boot up normally. The BIOS settings will be reset to their defaults.

11.3 Setting the Date and Time

The date and time are set in the BIOS. Select **Main** menu, then enter the date and time at the bottom of the screen. This screen also displays the CPU speed and memory capacity of the board.

11.4 Built-In Flash Drive with FreeDOS

Helios contains a built-in 8Mbit (2MB) flash memory pre-loaded with a ready to run copy of FreeDOS. This flash memory can be set up as a bootable A: drive. About 1.5MB of space is available for file storage.

To enable the flash drive, select the **Boot** menu, then **Boot Settings Configuration**. Scroll down to **OnBoard Virtual Flash FDD**, and select “External”. You can also write-protect the on-board flash drive to protect the files from being erased. To do this, select “External Read Only” instead of “External”. To ensure that write protection is not disabled later, you should assign a password to the BIOS using the **Security** menu.

To make the flashdisk the primary boot device, select the **Boot** menu. For **1st Boot Device**, select “SCSI Card”. Now the Helios can power up and boot to DOS without any attached storage device.

11.5 ISA Bus IRQ Reservation

An ISA bus IRQ must be reserved in the BIOS in order to be used by the on-board ISA bus circuits (serial ports and data acquisition) or an installed PC/104 module. To reserve an IRQ, go to the **PCIPnP** menu and scroll down to the IRQ list at the bottom. The default settings are: IRQ3, 4, 5, and 7 reserved, the remaining IRQs available.

11.6 Blue LED

Helios contains a programmable blue LED along the top edge of the board, near the VGA connector. This LED is controlled by the Vortex processor GPIO port 3 bit 4. It can be turned on and off in the BIOS and in software. The LED is on by default.

To turn the LED on or off in the BIOS, go to the **Chipset** menu, select **South Bridge Configuration**, and then **LED**. This will select the power-on state of the LED. To control the LED via software, write to GPIO port 3 bit 4. The direction control register for GPIO port 3 is preset by the BIOS and should not be disturbed.

```
outp(0x7B, inp(0x7B) & 0xEF); // clear bit 4 of port 3 to turn LED ON
outp(0x7B, inp(0x7B) | 0x10); // set bit 4 of port 3 to turn LED OFF
```

11.7 ISA Bus Speed

The ISA bus default speed is 8.3MHz. It can be set to 16.6MHz for increased performance. The number of wait states can also be modified for optimum performance. Not all add-on boards will support higher speed or different wait state settings. If your system does not behave reliably, reset the settings to their default values.

Parameter	*Default*	*Options*
ISA Bus Speed	8.3MHz	8.3MHz, 16.6MHz
ISA 16-Bit I/O Wait States	1	1 – 8
ISA 8-Bit I/O Wait States	4	1 – 8
ISA 16-Bit Memory Wait States	1	0 – 7
ISA 8-Bit Memory Wait States	4	1 – 8

11.8 Quiet / Quick Boot / Splash Screen

Quiet boot replaces the system status and configuration screen that appears during startup with a blank screen or custom splash screen (if available). Quick boot turns off memory test during startup to save time. To enable these features, go to the **Boot** menu, then select **Boot Settings Configuration**. Diamond can provide custom splash screens upon request from an image file no larger than 22KB in size.

11.9 Boot Priority

To select Boot devices and priority, go to the **Boot** menu and highlight the devices with the cursor and using ENTER select from the available devices. The order you wish them to be accessed is based on the number of the menu item (1st, 2nd, 3rd, 4th Boot Device). Only devices which are currently attached to the board will appear in the list of options. Therefore if you want to select a hard drive or USB device as the boot device, you must connect it to the CPU first, then boot up and enter the BIOS, then select it as a boot device. If this menu option does not appear on the screen, it means that the on-board flash drive is not enabled, and either no boot devices are attached or the CPU does not recognize any attached boot devices.

11.10 System Reset

Helios contains a reset controller to reset the system under defined conditions. Reset occurs when any of the following occurs.

- User causes reset with a ground contact on the *Reset-* input pin (connector J14 pin 2).
- Input voltage drops below 4.75V.

A system reset will also cause a reset on the ISA bus to reset any installed PC/104 modules. The ISA Reset signal is an active high pulse with a 200ms duration.

12. SERIAL PORTS AND SYSTEM CONSOLE

12.1 Overview

Helios contains four 16550-style asynchronous serial ports derived from the Vortex86 processor. Each port has 16-character transmit and receive FIFOs and is capable of transmitting at speeds of 9600, 19.2K, 38.4K, 57.6K, or 115.2Kbaud. The default settings for all ports are 115.2K, N, 8, 1.

Ports 1 and 2 can be jumper-configured for RS-232, RS-422, or RS-485, and ports 3 and 4 are fixed RS-232. The transceivers provide 15KV ESD protection. In RS-422 and RS-485 mode, 120 ohm line termination can be enabled by jumper. In RS-422 mode, receiver biasing can be jumper selected to force the inputs to an inactive state.

Console redirection is available on any one port, COM1 – 4. This feature enables keyboard input and character video output to be routed to one of the serial ports. Console operation can be configured in the BIOS to be enabled during POST (power on self test before the operating system loads), always on, or always off.

12.2 Serial port Configuration

The serial port settings can be configured in the BIOS menus. Select the **Chipset** menu, then **South Bridge Configuration**, then **Serial Port Configuration** to modify the address, IRQ level, speed, and protocol. The default settings are shown below.

Port	*I/O Address*	*IRQ*	*Speed*	*Protocol*
COM1	0x3F8	4	115200	RS-232
COM2	0x2F8	3	115200	RS-232
COM3	0x3E8	10	115200	RS-232
COM4	0x2E8	11	115200	RS-232

Helios Serial Port Default Configuration

The available options for each port are:

Address (hex): 3F8, 2F8, 3E8, 2E8, 3A8, 2A8, 100, 108

IRQ level: 3, 4, 9, 10, 11

Baud rate: 2400, 4800, 9600, 19,200, 38,400, 57,600, 115,200

Protocol: COM1 and COM2: RS-232, RS-422, RS-485

COM3 and COM4: RS-232 only

Each serial port requires 8 bytes of address space starting with the base address selected. So for example, an address of 3F8 means an address range of 3F8 – 3FF.

Be careful to select unique vales for each port. Selecting the same value for more than one port will cause a conflict and lead to unpredictable behavior.

12.3 Console Redirection to a Serial Port

In many applications without a local display and keyboard, it may be necessary to obtain occasional keyboard and monitor access to the CPU for configuration, file transfer, or other operations. Helios supports this activity by enabling keyboard input and character output onto a serial port, referred to as console redirection. In the Helios default BIOS configuration, console redirection is enabled on COM1 with settings of 115.2Kbaud, N, 8, 1 and is always enabled. These settings can be changed in the BIOS as described below.

A serial port on another PC can be connected to the console serial port on Helios with a null modem cable. A null modem cable has a DB9 female connector at each end and swaps the TX and RX signals from one end to the other, so that two DTE devices can communicate directly with each other. PC serial ports are normally configured for DTE pinout.

A terminal emulation program, such as HyperTerminal, running on the other computer can be used to establish the connection and communicate with Helios. The terminal program must be capable of transmitting special characters including F4 (some programs or configurations trap special characters).

There are three possible configurations for console redirection:

- POST-only): The console is enabled only during BIOS self-test during power-up; after the OS begins to load the console will be disabled and the serial port will be made available to the operating system.
- Always On (default setting: the console is always active and is not available to the operating system.
- Disabled: the console is never active, and the serial port is available to the operating system.

Console redirection is configured in the BIOS according to the following steps:

1. Enter the BIOS during power-up or reset. If you are using an attached keyboard, press **DEL**. If you are using console redirection, press **F4**.
2. Select the Advanced menu with the left/right arrow keys.
3. Select Console Redirection with the up/down arrow keys.
4. In Serial Port Number, select Disabled to disable the function, or select COM1, COM2, COM3, or COM4.

   NOTE: If you select Disabled, you will not be able to enter BIOS again during power-up through the serial port. To enter BIOS when console redirection is disabled, you must attach a keyboard and monitor to the board and follow the standard procedure by pressing **DEL** during boot.
5. For Console Type, select ANSI.
6. You can modify the baud rate and flow control settings if desired.
7. Exit the BIOS and save your settings.

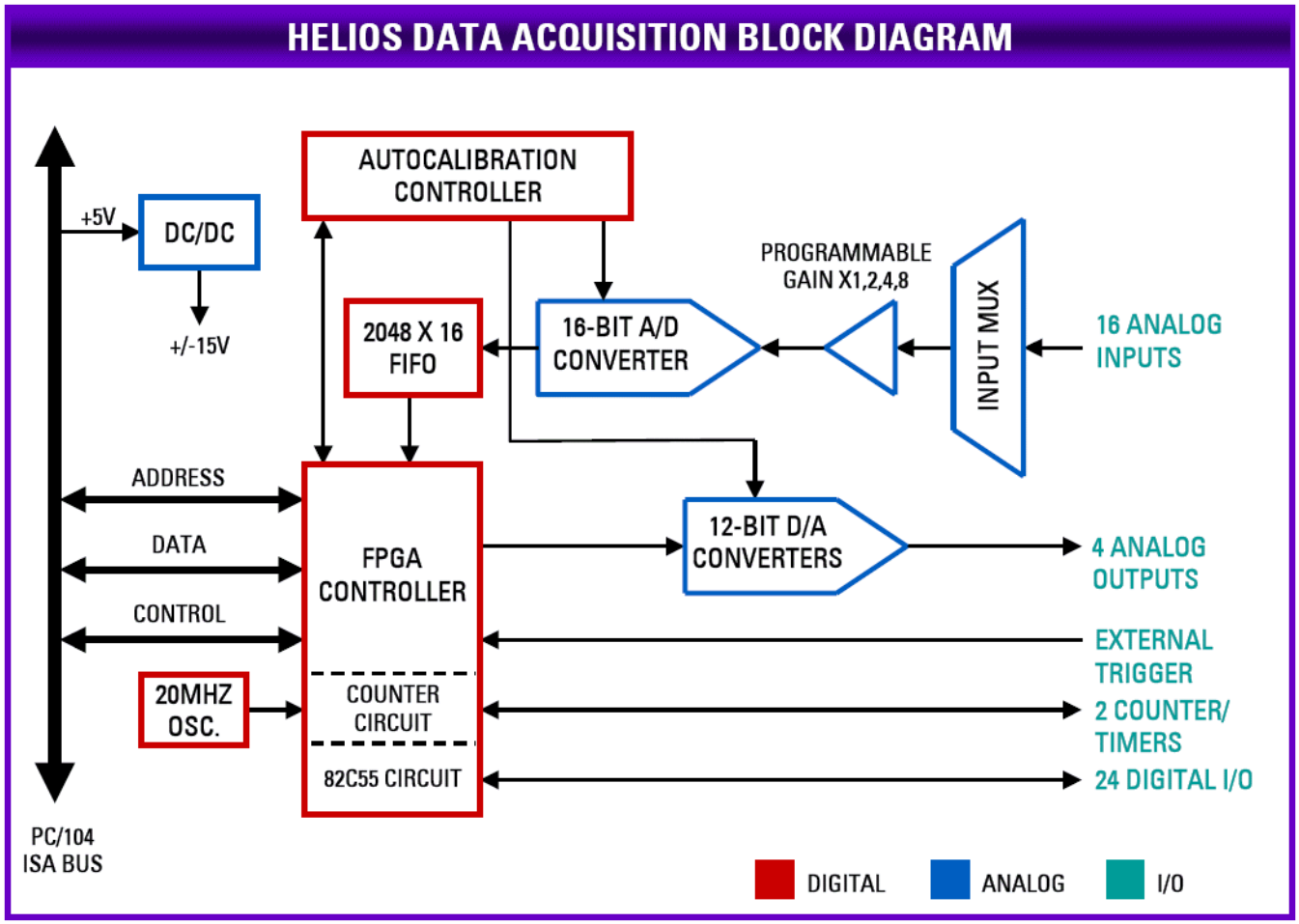
13. DATA ACQUISITION CIRCUIT OVERVIEW

Helios contains a data acquisition subsystem consisting of A/D, D/A, digital I/O, and counter/timer features. This subsystem is equivalent to a complete add-on data acquisition PC/104 module such as the Diamond Systems DMM-16-AT.

The A/D section includes a 16-bit A/D converter, 16 analog input channels, and a 2048-sample FIFO. Input ranges are programmable, and the maximum sampling rate is 250KHz. The D/A section includes 4 12-bit D/A channels. The digital I/O section includes up to 40 lines with programmable direction. The counter/timer section includes a 24-bit counter/timer to control A/D sampling rates and a 16-bit counter/timer for user applications.

High-speed A/D sampling is supported with interrupts and a FIFO. The FIFO is used to store up to 2048 A/D samples. An interrupt occurs when the FIFO reaches a user-selected threshold. Once the interrupt occurs, an interrupt routine runs and reads the data out of the FIFO. In this way the interrupt rate is reduced by a factor equal to the size of the FIFO threshold, enabling a faster A/D sampling rate and lower software overhead. The circuit can operate at sampling rates of up to 250KHz, with an interrupt rate of only 1KHz.

The A/D circuit uses the default settings of I/O address range 0x280 – 0x28F (base address 0x280) and IRQ 5. These settings can be changed if needed. The I/O address range is changed in the BIOS, and the interrupt level is changed with jumper block J21. The diagram below shows the Helios data acquisition circuit.



14. DATA ACQUISITION I/O REGISTER MAP

14.1 Overview

The data acquisition circuit on the AV model of Helios uses an FPGA which is attached to the ISA bus. It is accessible via a 16-byte window in ISA I/O space. It can be enabled or disabled in the BIOS. Select **Chipset**, then **South Bridge Configuration**, then **GPCS**. Select "Enabled" or "Disabled", and then select the desired base address. The default settings are Enabled and address = 280 (meaning 0x280 – 0x28F).

The available address options are: 200, 240, 280, 2C0, 300, 340, 380, 3C0

If the FPGA is disabled you will not be able to use the data acquisition circuit. The chosen address must not conflict or overlap with any other CPU feature or installed add-on board. Most Diamond I/O boards have a default I/O address of 300, so that address should not be used for the on-board data acquisition if a Diamond I/O board is installed.

The table below provides a high level overview of the register functions. Detailed bit by bit descriptions are in the next section.

Base +	Write Function	Read Function
	Main Registers	
0	Command	A/D LSB (bits 7-0)
1	Page Register	A/D MSB (bits 15-8)
2	A/D Channel Range	A/D Channel Range Read-back
3	A/D Gain and Scan Settings	A/D Gain Read-back, A/D & D/A status
4	Interrupt / Counter Control	Interrupt / Counter Control Read-back
5	FIFO Threshold	FIFO Threshold Read-back
6	D/A LSB	FIFO Current Depth / FIFO Status
7	D/A MSB / D/A Channel	Interrupt and A/D Channel Read-back
8	Digital I/O Port A Output	Digital I/O Port A Input
9	Digital I/O Port B Output	Digital I/O Port B Input
10	Digital I/O Port C Output	Digital I/O Port C Input
11	Digital I/O / DA Control	Digital I/O / DA Control Read-back
	Page 0: Counter/Timers	
12	Counter/Timer 0/1 D7-0	Counter/Timer 0/1 D7-0
13	Counter/Timer 0/1 D15-8	Counter/Timer 0/1 D15-8
14	Counter/Timer 0 D23-16	Counter/Timer 0 D23-16
15	Counter/Timer Control	FPGA Revision Code
	Page 1: Autocalibration Control	
12	EEPROM/TrimDAC data latch	EEPROM/TrimDAC data read-back
13	EEPROM/TrimDAC address latch	EEPROM/TrimDAC address read-back
14	EEPROM/TrimDAC control register	EEPROM/TrimDAC status register
15	EEPROM Access Code	
	Page 2: Expanded FIFO, A/D & D/A Configuration	
12	Expanded FIFO depth register	Expanded FIFO depth read-back
13	AD Mode Configuration	AD Mode Configuration Read-back
14	DA Mode Configuration	DA Mode Configuration Read-back
15	DA MSB (16-bit Mode)	DA Simultaneous Update

14.2 Register Write Functions

Base +	7	6	5	4	3	2	1	0
Main Registers								
0	STARTAD	RSTBRD	RTSDA	RSTFIFO	-	CLRT	CLRD	CLRA
1	-	-	-	-	-	-	PG1	PG0
2	H3	H2	H1	H0	L3	L2	L1	L0
3	-	-	-	-	-	SCANEN	ADG1	ADG0
4	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	-	TINTE	DINTE	AINTE
5	-	-	FT5	FT4	FT3	FT2	FT1	FT0
5(*)	FT10	FT09	FT08	FT07	FT06	FT05	FT04	FT03
6	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
7	DACH1	DACH0	-	-	DA11	DA10	DA9	DA8
8	A7	A6	A5	A4	A3	A2	A1	A0
9	B7	B6	B5	B4	B3	B2	B1	B0
10	C7	C6	C5	C4	C3	C2	C1	C0
11	DIOCTR	DAMODE	DASIM	DIRA	DIRCH	-	DIRB	DIRCL
Page 0: Counter/Timer Access								
12	CtrD7	CtrD6	CtrD5	CtrD4	CtrD3	CtrD2	CtrD1	CtrD0
13	CtrD15	CtrD14	CtrD13	CtrD12	CtrD11	CtrD10	CtrD9	CtrD8
14	CtrD23	CtrD22	CtrD21	CtrD20	CtrD19	CtrD18	CtrD17	CtrD16
15	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR
Page 1: AutoCal Control								
12	D7	D6	D5	D4	D3	D2	D1	D0
13	A7	A6	A5	A4	A3	A2	A1	A0
14	EE_EN	EE_RW	RUNCAL	CALMUX	TDACEN	-	-	-
15	EEPROM Access Key Register							
Page 2: Expanded FIFO and AD/DA Control								
12	-	-	-	-	-	-	-	EXFIFO
13	-	-	-	-	ADPOL	-	ADSD	-
14	DAUR	-	DACH1	DACH0	DAPOL	-	DAG1	DAG0
15	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

(*) During Enhanced FIFO mode (EXFIFO=1)

14.3 Register Read Functions

Base +	7	6	5	4	3	2	1	0
Main Registers								
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	H3	H2	H1	H0	L3	L2	L1	L0
3	ADBUSY	SE/DIFF	ADWAIT	DACBSY	OF	SCANEN	ADG1	ADG0
4	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	-	TINTE	DINTE	AINTE
5	-	-	FT5	FT4	FT3	FT2	FT1	FT0
5(*)	FD07	FD06	FD05	FD04	FD03	FD02	FD01	FD00
6	-	-	FD5	FD4	FD3	FD2	FD1	FD0
6(*)	FD11	FD10	FD09	FD08	OF	FF	HF	EF
7	-	TINT	DINT	AINT	ADCH3	ADCH2	ADCH1	ADCH0
8	A7	A6	A5	A4	A3	A2	A1	A0
9	B7	B6	B5	B4	B3	B2	B1	B0
10	C7	C6	C5	C4	C3	C2	C1	C0
11	DIOCTR	DAMODE	DASIM	DIRA	DIRCH	-	DIRB	DIRCL
Page 0: Counter/Timer Access								
12	CtrD7	CtrD6	CtrD5	CtrD4	CtrD3	CtrD2	CtrD1	CtrD0
13	CtrD15	CtrD14	CtrD13	CtrD12	CtrD11	CtrD10	CtrD9	CtrD8
14	CtrD23	CtrD22	CtrD21	CtrD20	CtrD19	CtrD18	CtrD17	CtrD16
15	FPGA Revision Code							
Page 1: AutoCal Control								
12	D7	D6	D5	D4	D3	D2	D1	D0
13	A7	A6	A5	A4	A3	A2	A1	A0
14	-	TDBUSY	EEBUSY	CALMUX	-	-	-	-
15	Not Used							
Page 2: Expanded FIFO and AD/DA Control								
12	-	-	-	-	-	-	-	EXFIFO
13	DAUR	DACH1	DACH0	-	ADPOL	-	ADSD	-
14	-	-	-	DASIZE	DAPOL	-	DAG1	DAG0
15	D/A Simultaneous Update							

(*) During Enhanced FIFO mode (EXFIFO=1)

14.4 I/O Map Detailed Description

In all register definitions below, a bit named 'X' or '-' is not defined and serves no function. On readback any such bit will read as a 0.

14.4.1 Main Registers

Base + 0 Write Command Register

Bit No.	7	6	5	4	3	2	1	0
Name	STRTAD	RSTBRD	RSTDA	RSTFIFO	-	CLRT	CLRD	CLRA

This register is used to perform various functions. The register bits are not data bits but instead command triggers. Each function is initiated by writing a 1 to a particular bit. Writing a 1 to any bit in this register does not affect any other bit in this register. For example, to reset the FIFO, write the value 0x10 (16) to this register to write a 1 to bit 4. No other function of the register will be performed. Multiple actions can be carried out simultaneously by writing a 1 to multiple bits simultaneously.

STRTAD Writing a 1 to this bit starts an A/D conversion (trigger the A/D) when in software-trigger mode (AINTE = 0). The A/D conversion will start and the ADBUSY bit (base+3, bit 7) will go high. When the A/D conversion completes and the data is stored in the FIFO, the STS bit goes low.

When AINTE = 1 (base+4, bit 0), the A/D cannot be triggered by writing to this bit. Instead the A/D will be triggered by a signal selected by ADCLK (base+4, bit 5).

RSTBRD Writing a 1 to this bit will reset the entire board excluding the D/A, causing all registers on the board to be reset to 0. The effect on the digital I/O is that all ports are reset to input mode, and the logic state of their pins will be determined by the pull-up/pull-down configuration setting selected by the user. All A/D, counter/timer and interrupt functions will cease. However the D/A values will remain constant.

RSTDA Writing a 1 to this bit causes the FPGA to send a reset command to the D/A converter.

RSTFIFO Reset the FIFO depth to 0. This clears the FIFO so that further A/D conversions will be stored in the FIFO starting at address 0. All FIFO flags are set to their states for empty FIFO (EF = 1, all others = 0).

CLRT Writing a 1 to this bit causes the timer interrupt request flip flop to be reset.

CLRD Writing a 1 to this bit causes the digital I/O interrupt request flip flop to be reset.

CLRA Writing a 1 to this bit causes the analog interrupt request flip flop to be reset.

Base + 0 Read A/D LSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

If the FIFO is not empty, this register returns the LSB of the A/D value stored at the current FIFO pointer. If the FIFO is empty, reading from this register returns 0.

AD7 – 0 A/D data bits 7 - 0; AD0 is the LSB.

Base + 1 Write Page Register

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	PG1	PG0

PG1-PG0 Page Select (0 - 2): The addresses base+12 to base+15 provide a window into 3 pages of registers, 0-2. Page 3 is undefined and maps back to page 0.

Base + 1 Read A/D MSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

If the FIFO is not empty, this register returns the MSB of the A/D value stored at the current FIFO pointer and decrements the FIFO depth value by 1 sample. If the FIFO is empty, reading from this register returns 0.

AD15 - 8 A/D data bits 15 – 8; AD15 is the MSB.

Base + 2 Read/Write A/D Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name	H3	H2	H1	H0	L3	L2	L1	L0

When this register is written to, the current A/D channel is set to the channel specified by L3-0, so that the next time an A/D conversion is triggered the channel specified by L3-0 will be sampled.

When this register is written to, the WAIT bit (base+3, bit 5) will go high for 10 microseconds to indicate that the analog input circuit is settling. During this time the board will ignore any A/D start command. It is still possible to write to base+3 to configure the analog input circuit during the WAIT period. In this case the WAIT delay is retriggered, so that it will always endure for the full wait period after the last triggering function.

The A/D circuit is designed to automatically increment the A/D channel each time an A/D conversion is triggered. This enables the user to avoid having to write the A/D channel each time. The A/D channel will rotate through the values between L3-0 and H3-0. When channel H3-0 is sampled, the register resets to L3-0.

Reading from this register returns the value previously written to it.

H3 – H0 High channel of channel scan range (HIGH)

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

L3 - L0 Low channel of channel scan range (LOW)

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

It is not required that the High channel be greater or equal to the Low channel. A setting of Low=14 and High=2 is valid. In this case the channel sequence is 14, 15, 0, 1, 2, 14, 15, …

Base + 3 Write Analog Input Gain and Scan Control

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	SCANEN	ADG1	ADG0

When this register is written to, the WAIT bit (base+3, bit 5) will go high for 10 microseconds to indicate that the analog input circuit is settling. During this time the board will ignore any A/D start command. It is still possible to write to base+2 to configure the analog input channel register during the WAIT period. In this case the WAIT delay is retriggered, so that it will always endure for the full wait period after the last triggering function.

SCANEN Scan mode enable:

1 Each A/D trigger to cause the board to generate an A/D conversion on each channel in the range LOW – HIGH as defined in Base+2. The ADBUSY bit (base+3, bit 7) stays high during the entire scan.

0 Each A/D trigger to cause the board to generate a single A/D conversion on the current channel. The internal channel pointer will increment to the next channel in the range LOW – HIGH or reset to LOW if the current channel is HIGH. The ADBUSY bit stays high during the A/D conversion.

ADG1-0 Analog input gain. The gain is the ratio of the voltage seen by the A/D converter and the voltage applied to the input pin. The gain setting is the same for all input channels. The following table lists the available analog input ranges. Unipolar / bipolar range is selected with the ADPOL bit in page 2 base+13.

ADG1	ADG0	Gain	Unipolar Range	Bipolar Range
0	0	1	0-10V	±10V
0	1	2	0-5V	±5V
1	0	4	0-2.5V	±2.5V
1	1	8	0-1.25V	±1.25V

Base + 3 Read Analog Input Status

Bit No.	7	6	5	4	3	2	1	0
Name	ADBUSY	SE/DIFF	ADWAIT	DACBSY	OF	SCANEN	ADG1	ADG0

ADBUSY A/D Busy. 1 = A/D conversion or scan in progress, 0 = A/D is idle.

After starting a conversion in software, the program must monitor ADBUSY and wait for it to become 0 prior to reading A/D values. If SCANEN = 0 (single conversion mode), ADBUSY goes high when an A/D conversion is started and stays high until the conversion is finished. If SCANEN = 1 (scan mode enabled), ADBUSY stays high during the entire scan.

SE/DIFF Single-ended / Differential mode indicator. 0 = Single-ended, 1 = Differential.

ADWAIT A/D input circuit status. 1 = A/D circuit is settling on a new value, 0 = ok to start conversion.

ADWAIT goes high after the channel register (base+2) or the gain register (base+3) is changed. It stays high for 10 microseconds. The program should monitor this bit after writing to either register and wait for it to become 0 prior to starting an A/D conversion.

DACBSY Indicates the DAC is busy updating (approx. 4 µS). 1 = Busy, 0 = Idle. Any writes to the DAC (base+6, base+7, or page 2 base+15) while DACBSY = 1 will be ignored.

OF FIFO Overflow bit. This bit indicates that the FIFO has overflowed, meaning that the A/D circuit has attempted to write data to it when it is full.

When overflow occurs, the FIFO will not accept any more data until it is reset. Once set, the OF flag remains true until the FIFO is reset, so the application program will be able to determine if overflow has occurred. If overflow occurs, then you must either reduce the sample rate or increase the efficiency of your interrupt routine and/or operating system.

SCANEN, ADG1-0 Readback of scan enable and A/D gain settings written to base+2

Base + 4 Read/Write Interrupt / Counter Control

Bit No.	7	6	5	4	3	2	1	0
Name	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	-	TINTE	DINTE	AINTE

Analog output interrupts are not supported on this board.

Multiple interrupt operations may be performed simultaneously. All interrupts will be on the same interrupt level. The user's interrupt routine must monitor the status bits to know which circuit has requested service. After processing the data but before exiting, the interrupt routine must then clear the appropriate interrupt request bit using the register at base+0.

CKSEL1 Clock source selection for counter/timer 1:

0 = internal oscillator, frequency selected by FRQSEL1

1 = external clock input CLK1 (DIOCTR must be set to 1 to enable CLK1 input on J17)

FRQSEL1 Input frequency selection for counter/timer 1 when CKSEL1 = 1:

0 = 10MHz

1 = 100KHz

FRQSEL0 Input frequency selection for counter/timer 0.

0 = 10MHz

1 = 1MHz

ADCLK A/D trigger select when AINTE = 1:

0 = internal clock output from counter/timer 0

1 = external signal on pin 25 of the analog I/O connector J17.

TINTE Enable timer interrupts: 1 = enable, 0 = disable

DINTE Enable digital I/O interrupts: 1 = enable, 0 = disable

AINTE Enable analog input interrupts: 1 = enable, 0 = disable

When AINTE = 0. the A/D is triggered only by writing a 1 to the ADSTART bit at base+0.

When AINTE = 1, the A/D cannot be triggered by setting the ADSTART bit at base+0. Instead the A/D trigger comes from the hardware source selected by the ADCLK bit.

Base + 5 Write FIFO Threshold / FIFO Threshold X8

Basic Mode: EXFIFO = 0 (See Register Description for page 2, base+12)

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	FT5	FT4	FT3	FT2	FT1	FT0

FT5–0 FIFO threshold. When the number of A/D samples in the FIFO reaches this number, the board will generate an interrupt and set AINT high (base+7, bit 4) when AINTE=1.

The valid range is 1-48. If the value written is greater than 48, then 48 will be used. If the value written is 0, then 1 will be used.

Enhanced Mode: EXFIFO = 1 (See Register Description for page 2, base+12)

Bit No.	7	6	5	4	3	2	1	0
Name	FT10	FT09	FT08	FT07	FT06	FT05	FT04	FT03

FT10–03 FIFO threshold (upper 8 of 11 bits). The lower 3 bits are 000. The FIFO threshold will be set to 8x the number programmed into this register (left shift 3 bits). When the number of A/D samples in the FIFO reaches the threshold, the board will generate an interrupt and set AINT high (base+7, bit 4) when AINTE=1.

The valid range is 1 – 255, corresponding to a FIFO threshold of 8-2040.

When EXFIFO is set to 1 the FIFO threshold is set automatically to 1024.

Base + 5 Read FIFO Threshold / FIFO Depth LSB

Basic Mode: EXFIFO = 0 (See Register Description for page 2, base+12)

Bit No.	7	6	5	4	3	2	1	0
Name	0	0	FT5	FT4	FT3	FT2	FT1	FT0

FT5-0 Readback of the programmed FIFO threshold value

Enhanced Mode: EXFIFO = 1 (See Register Description for page 2, base+12)

Bit No.	7	6	5	4	3	2	1	0
Name	FD07	FD06	FD05	FD04	FD03	FD02	FD01	FD00

FD07-00 FIFO depth. Readback of the lower 8 bits of the number of A/D values currently stored in the FIFO.

Base + 6 **Write** **DAC LSB**

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA7–0 D/A data bits 7 - 0; This register stores the DA LSB in both 12 and 16-bit modes.

Base + 6 **Read** **A/D Channel and FIFO Status**

Basic Mode: EXFIFO = 0 (See Register Description for page 2, base+12)

Bit No.	7	6	5	4	3	2	1	0
Name	0	0	FD5	FD4	FD3	FD2	FD1	FD0

FD5–0 FIFO depth. Readback of the number of A/D values currently stored in the FIFO.

Enhanced Mode: EXFIFO = 1 (See Register Description for page 2, base+12)

Bit No.	7	6	5	4	3	2	1	0
Name	FD11	FD10	FD09	FD08	OF	FF	HF	EF

FD11–08 Readback of the upper 4 bits of the number of A/D values currently stored in the FIFO.

OF FIFO Overflow flag.

1 = FIFO has overflowed, meaning that the A/D circuit has attempted to write data to it when it is full. The OF flag is set whenever FF = 1 and an A/D conversion completes (STS goes high then low).

0 = FIFO has not overflowed.

FF FIFO Full Bit.

0 = FIFO is not full; the FIFO is able to accept data from the A/D circuit.

1 = FIFO is full; the next conversion will result in an overflow.

HF FIFO Half Full Bit.

0 = the FIFO is less than half full.

1 = the FIFO is half full or greater.

EF FIFO Empty.

0 = the FIFO still has data.

1 = the FIFO is empty.

Base + 7 Write DAC MSB

Bit No.	7	6	5	4	3	2	1	0
Name	DACH1	DACH0	-	-	DA11	DA10	DA9	DA8

When this register is written, the D/A channel selected by DACH1-0 will be loaded using the currently stored D/A value in the registers selected by DAMODE. If DASIM=0, the D/A will then be updated. If DASIM=1, the D/A will not be updated.

DACH1–0 D/A channel, 0-3.

DA11–8 D/A bits 11 – 8 when operating the D/A in 12-bit mode. These bits are ignored for 16-bit mode.

Base + 7 Read Analog Operation Status

Bit No.	7	6	5	4	3	2	1	0
Name	-	TINT	DINT	AINT	ADCH3	ADCH2	ADCH1	ADCH0

When any of the bits 6–4 are 1, the corresponding circuit is requesting interrupt service. The interrupt routine must poll these bits to determine which circuit needs service and then act accordingly.

TINT Timer interrupt status: 1 = interrupt pending, 0 = interrupt not pending.

DINT Digital I/O interrupt status: 1 = interrupt pending, 0 = interrupt not pending.

AINT Analog input interrupt status: 1 = interrupt pending, 0 = interrupt not pending.

ADCH3-0 Current A/D channel. This is the channel that will be sampled on the **next** A/D conversion.

Base + 8 Read / Write Digital I/O Port A

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0

This register is used for digital I/O on port A. When port A is in output mode, the output pins DIO A7-0 on data acquisition connector J17 will be set to the values in this register, and reading this register will read back the programmed value. When port A is in input mode, this register will read back the logic levels on pins DIO A7-0, and writing to this register will have no effect. The direction of port A is controlled by the DIO control register at base+11.

Base + 9 Read / Write Digital I/O Port B

Bit No.	7	6	5	4	3	2	1	0
Name	B7	B6	B5	B4	B3	B2	B1	B0

This register is used for digital I/O on port B. When port B is in output mode, the output pins DIO B7-0 on data acquisition connector J17 will be set to the values in this register, and reading this register will read back the programmed value. When port B is in input mode, this register will read back the logic levels on pins DIO B7-0, and writing to this register will have no effect. The direction of port B is controlled by the DIO control register at base+11.

Base + 10 Read / Write Digital I/O Port C

Bit No.	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0

This register is used for digital I/O on port C. It operates in similar fashion to ports A and B, except that 4 pins on the I/O connector serve a different purpose based on the value of DIOCTR in base+11.

When DIOCTR=0, the behavior is as follows: When port C is in output mode, the output pins DIO C7-0 on data acquisition connector J17 will be set to the values in this register, and reading this register will read back the programmed value. When port C is in input mode, this register will read back the logic levels on pins DIO C7-0, and writing to this register will have no effect. The direction of port C is controlled by the DIO control register at base+11.

When DIOCTR=1, the behavior of bits C3-0 is the same as above, and bits C7-4 are not functional. Instead, the corresponding I/O pins on connector J17 are used for counter/timer signals as described in base+11 below.

Base + 11 Read / Write Digital I/O and D/A Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	DIOCTR	DAMODE	DASIM	DIRA	DIRCH	-	DIRB	DIRCL

DIOCTR Selects counter I/O signals or digital I/O lines on 4 pins on the data acquisition I/O connector J17:

J17 Pin No.	DIOCTR = 1	DIOCTR = 0
21	Gate 0	DIO C4
22	Gate 1	DIO C5
23	Clk 1	DIO C6
24	Out 0	DIO C7

If DIOCTR = 0, then the direction of these pins is controlled by DIRCH.

DAMODE 16/12-bit DAC mode. This bit should only be set for custom models of Helios with a 16-bit DAC installed. This bit defines where the high bits of the D/A value are to be found when loading the D/A. Regardless of whether the installed D/A is 12 bits or 16 bits, the data value written to the D/A is always 16 bits in length. For a 12-bit D/A, the 12-bit data is left-justified in this 16-bit word, and the lowest 4 bits are always 0000.

0 D/A is being used in 12-bit mode (standard configuration). The data register at Base+5 contains the high bits 11-8 of the 12-bit D/A value.

1 D/A is being used in 16-bit mode (custom configuration). The data register at Page 2 Base+15 contains the high bits 15-8 of the 16-bit D/A value.

DASIM D/A simultaneous update control. This bit determines when the D/A is updated.

0 When Base+6 is written, the D/A data is loaded into the D/A and the update command is sent immediately afterwards.

1 When Base+6 is written, the 12/16-bit values will be loaded into the D/A converter but the update command will not be issued. Instead, a read of the register at Page 2, Base+15 will cause the update of the D/A converter.

DIRA Port A direction. 0 = output, 1 = input

DIRB Port B direction: 0 = output, 1 = input

DIRCH Port C bits 7-4 direction: 0 = output, 1 = input. This bit has no effect if DIOCTR=1.

DIRCL Port C bits 3-0 direction: 0 = output, 1 = input

14.4.2 Page 0: Counter/Timer Control

Page 0, Base + 12 Read/Write Counter/Timer 0/1 D7 - 0

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0

This register is used for both Counter 0 and Counter 1. It is the LSB for both counters.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through page 0, base + 15, the selected counter's LSB register will be loaded with this value.

When reading from this register, the LSB value of the most recent Latch command will be returned. The value returned is NOT the value written to this register.

Page 0, Base + 13 Read/Write Counter/Timer 0/1 D15 - 8

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8

This register is used for both Counter 0 and Counter 1. It is the MSB for counter 1 and the middle byte for counter 0.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through page 0, base + 15, the selected counter's associated register will be loaded with this value. For counter 0, it is the middle byte. For counter 1, it is the MSB.

When reading from this register, the associated byte of the most recent Latch command will be returned. The value returned is NOT the value written to this register.

Page 0, Base + 14 Read/Write Counter/Timer 0 D23 - 16

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16

This register is used for Counter 0 only. Counter 0 is 24 bits wide, while Counter 1 is only 16 bits wide.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through page 0, base+15 for Counter 0, the counter's MSB register will be loaded with this value. When issuing a Load command for counter 1, this register is ignored.

When reading from this register, the associated byte of the most recent Latch command will be returned. The value returned is NOT the value written to this register.

Page 0, Base + 15 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

This register is used to control the counter/timers. A counter is selected with bit 7, and then a 1 is written to any ONE of bits 6 – 0 to select the desired operation for that counter. The other bits and associated functions are not affected. Only one operation can be performed at a time. If more than one of bits 6-0 is set simultaneously, the highest numbered bit will determine the operation to be performed.

CTRNO Counter no., 0 or 1

LATCH Latch the selected counter so that its value may be read. The counter must be latched before it is read. Reading from registers at page 0, base+12 thru base+14 returns the most recently latched value. If you are reading Counter 1 data, read only page 0, base+12 and base+13. Any data in page 0, base+14 will be from the previous Counter 0 access.

GTDIS Disable external gating for the selected counter (see GTEN below).

GTEN Enable external gating for the selected counter. If enabled, the associated input signal GATE0 or GATE1 controls counting on the counter. If the GATEn signal is high, counting is enabled. If the GATEn signal is low, counting is disabled.

CTDIS Disable counting on the selected counter. The counter will ignore input pulses.

CTEN Enable counting on the selected counter. The counter will decrement on each input pulse.

LOAD Load the selected counter with the data written to page 0, base+12 through base+14 (Counter 0) or page 0, base+12 and base+13 (Counter 1).

CLR Clear the current counter (set its value to 0). Counter operation such as count enable or gate enable is not affected by the CLR command. If the counter is enabled it will continue to count input pulses.

Page 0, Base + 15 Read FPGA Revision Code

Bit No.	7	6	5	4	3	2	1	0
Name	BID3	BID2	BID1	BID0	REV3	REV2	REV1	REV0

This register is used to indicate the board ID and data acquisition FPGA revision. The initial production version of Helios reads back ID code 0x70. The code will increment by 1 each time a new revision is released.

REV3-0 Revision code. This reads back as 0 in the initial production release of the on-board FPGA code and increments by 1 for each subsequent update.

BID3-0 Board ID code. This reads back as 7 (b0111) for Helios.

14.4.3 Page 1: AutoCalibration Control

Page 1, Base + 12 Read/Write EEPROM / TrimDAC Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

During EEPROM or TrimDAC write operations, the data written to this register will be written to the selected device.

During EEPROM read operations this register contains the data to be read from the EEPROM and is valid after EEBUSY = 0.

The TrimDAC data cannot be read back.

D7-0 Calibration data to be read or written to the EEPROM and/or TrimDAC.

Page 1, Base + 13 Read/Write EEPROM / TrimDAC Address Register

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0

A7-A0 EEPROM / TrimDAC address.

The EEPROM recognizes address 0 – 255 using address bits A7 – A0. The TrimDAC only recognizes addresses 0 – 7 using bits A2 – A0. In each case remaining address bits will be ignored.

Page 1, Base + 14 Write Calibration Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	EE_EN	EE_RW	RUNCAL	CALMUX	TDACWR	X	X	X

This register is used to initiate various commands related to autocalibration.

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit. If both EE_EN and TDACWR are set to '1' then TDACWR is ignored.

EE_RW Selects read or write operation for the EEPROM:

0 = Write

1 = Read

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM. If this bit is set to 1, all other bits written to this register are ignored, however the current value of CALMUX is preserved.

CALMUX Calibration multiplexor enable. The cal mux is used to read precision on-board reference voltages that are used in the autocalibration process. It also can be used to read back the value of analog output 0.

1 = enable cal mux and disable user analog input channels

0 = disable cal mux, enable user inputs

TDACWR TrimDAC Write. Writing 1 to this bit will initiate a transfer to the TrimDAC addressed by the register at page 1, base+13. (used in the autocalibration process). If both EE_EN and TDACWR are set to '1' then TDACWR is ignored.

Page 1, Base + 14 Read Calibration Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	0	TDBUSY	EEBUSY	CALMUX	0	0	0	0

TDBUSY TrimDAC busy indicator.

0 User may access TrimDAC

1 TrimDAC is being accessed; user must wait.

EEBUSY EEPROM busy indicator.

0 User may access EEPROM

1 EEPROM is being accessed; user must wait.

CALMUX Readback of calibration multiplexor enable setting:

1 Enabled.

0 Disabled.

Page 1, Base + 15 Write EEPROM Access Key Register

The user must write the key value 0xA5 (binary 10100101) to this register each time after any change in the states of registers bits PG1 and PG0 (base+1 bits 1-0) in order to get access to the EEPROM. This helps prevent accidental corruption of the EEPROM contents. Once the key value is written, access to the EEPROM remains enabled until the page bits are changed.

14.4.4 Page 2 Expanded FIFO and AD/DA Control

Page 2 Base + 12 Read/Write Expanded FIFO Control

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	EXFIFO

EXFIFO Expanded FIFO enable. Default and reset value is 0.

0 The FIFO is set in basic mode and the registers at base+5 and base+6 are in basic mode. The FIFO size is set to 48 samples and the threshold is set to 24.

1 The FIFO is set in enhanced mode, and the registers at base+5 and base+6 are in enhanced mode. The FIFO size is set to 2048 samples and the threshold is set to 1024.

Page 2 Base + 13 Read/Write AD Mode Configuration

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	ADPOL	-	ADSD	-

This register functions as an AD configuration jumper override for the DAQ subsection. This register resets to zero on power-up or reset.

ADPOL A/D polarity configuration:

0 Bipolar operation

1 Unipolar operation

ADSD A/D single-ended / differential configuration:

0 Single-ended operation

1 Differential operation

Page 2 Base + 14 Write DA Mode Configuration

Bit No.	7	6	5	4	3	2	1	0
Name	DAUR	-	DARCH1	DARCH0	DAPOL	-	DAG1	DAG0

This register defines the D/A output range. The control data sent to the D/A chip contains a 4 bit range / command instruction S3-0, whose value is defined based on the bits in this register according to the table below. When this register is written, the range command will be sent to the D/A according to the logic described here.

DAUR DA unique range:

0 All D/A channels receive the same range selected by DAPOL and DAG1-0.

1 Only the D/A channel indicated by DACH1-0 should be set to the range selected by DAPOL and DAG1-0.

DARCH1-0 DA channel for selected range. If DAUR=0, these bits are ignored. If DAUR=1, these bits determine which D/A channel will have the range programmed according to DAPOL and DAG1-0.

DAPOL D/A polarity configuration

DAG1-0 D/A converter output range

DAPOL	DAG1	DAG0	DAC control bits				DAC output range or function
			S3	S2	S1	S0	
0	0	0	0	0	0	0	0 to 5V (unipolar 5V span)
1	0	0	0	1	0	0	±2.5V (bipolar 5V span)
0	0	1	0	0	0	1	0 to 10V (unipolar 10V span)
1	0	1	0	0	1	0	±5V (bipolar 10V span)
0	1	0	0	0	0	0	Not Used – Setting Ignored
1	1	0	0	0	1	1	±10V (bipolar 20V span)
X	1	1	0	0	0	0	D/A converter shut down

Page 2 Base + 14 **Read** **DA Mode Configuration**

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	DASIZE	DAPOL	-	-	-

DASIZE This bit indicates the resolution of the D/A converter installed. The standard models of Helios all use a 12-bit DAC.

0 12-bit DAC

1 16-bit DAC

Page 2 Base + 15 **Write** **DAC MSB – 16-Bit Enhanced Mode**

Bit No.	7	6	5	4	3	2	1	0
Name	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

When DAMODE=1 (base+11 bit 6), the value written to this register forms the upper 8 bits of the 16-bit D/A value that is written to the D/A. When DAMODE=0, this register is ignored. This behavior is consistent regardless of the DASIZE value. DAMODE=1 should only be used when the 16-bit DAC is installed. The standard models of Helios use the 12-bit DAC.

DA15–8 D/A data bits 15 - 8; DA15 is the MSB.

Page 2 Base + 15 **Read** **D/A Simultaneous Update**

If DA simultaneous update is enabled (DASIM=1), reading this register will update the DAC outputs in both 12 and 16-bit mode. The value read back is 0.

15. ANALOG-TO-DIGITAL INPUT RANGES AND RESOLUTION

15.1 Overview

The Helios AV model data acquisition circuit uses a 16-bit A/D converter. The full range of numerical values for a 16-bit number is 0 - 65535. However, the A/D converter uses two's complement notation, so the A/D value is communicated as a signed integer, ranging from -32768 to +32767. Regardless of whether the A/D is configured for unipolar or bipolar input ranges, the value -32768 always refers to the bottom of the input range, and the value 32767 always refers to the top.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and is referred to as 1 LSB (1 Least Significant Bit). The resolution is always 16 bits, but the value of 1 LSB will vary with the input range.

15.2 Input Range Selection

You can select a gain setting for the inputs, which causes them to be amplified before they reach the A/D converter. The gain setting is controlled in software and can be changed anytime, so that you can use different gains for different input signals. In general, you should select the highest gain (smallest input range) that allows the A/D converter to read the full range of voltages over which the input signals will vary. However, a gain that is too high causes the A/D converter to clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

The table below indicates the available analog input ranges. The polarity is set with bit ADPOL at page 2 base+13 bit 3, and the gain is set with the G1 and G0 bits in the register at base+3. The Gain value in the table is provided for clarity. The single-ended vs. differential setting (ADSD) has no impact on the input range or the resolution.

Polarity	*Gain*	*ADPOL*	*G1*	*G0*	*Input Range*	*Resolution (1LSB)*
Bipolar	1	0	0	0	±10V	305µV
Bipolar	2	0	0	1	±5V	153µV
Bipolar	4	0	1	0	±2.5V	76µV
Bipolar	8	0	1	1	±1.25V	38µV
Unipolar	1	1	0	0	0 - 10V	153µV
Unipolar	2	1	0	1	0 - 5V	76µV
Unipolar	4	1	1	0	0 - 2.5V	38µV
Unipolar	8	1	1	1	0 - 1.25V	19µV

16. PERFORMING AN A/D CONVERSION

16.1 Introduction

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (without the driver software). Perform an A/D conversion according to the following steps. Each step is discussed in detail below.

1. Select the input channel range.
2. Select the input range and scan option.
3. Select the polarity.
4. Wait for analog input circuit to settle.
5. Initiate an A/D conversion.
6. Wait for the conversion to finish.
7. Read the data from the board.
8. Convert the numerical data to volts or engineering units.

The control registers associated with A/D conversions are provided below for reference:

Base +	R/W	7	6	5	4	3	2	1	0
Main Registers									
0	W	**STARTAD**	RSTBRD	RTSDA	RSTFIFO	-	CLRT	CLRD	CLRA
0	R	**AD7**	**AD6**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**
1	W	-	-	-	-	-	-	**PG1**	**PG0**
1	R	**AD15**	**AD14**	**AD13**	**AD12**	**AD11**	**AD10**	**AD9**	**AD8**
2	R/W	**H3**	**H2**	**H1**	**H0**	**L3**	**L2**	**L1**	**L0**
3	W	-	-	-	-	-	**SCANEN**	**ADG1**	**ADG0**
3	R	**ADBUSY**	SE/DIFF	**ADWAIT**	DACBSY	OF	**SCANEN**	**ADG1**	**ADG0**
Page 2: FIFO and AD/DA Control									
13	R/W	-	-	-	-	**ADPOL**	-	**ADSD**	-

STARTAD Write a 1 to this bit to start an A/D conversion or scan

AD15-0 A/D data value

PG1-0 Selects page 0, 1, or 2 at addresses base+12 through base+15

H3-0 High channel of selected A/D channel range

L3-0 Low channel of selected A/D channel range

SCANEN A/D scan enable: 0 = single sample each trigger, 1 = scan of all channels each trigger

ADG1-0 A/D gain setting, see table in section 15.2

ADBUSY A/D busy indicator: 0 = A/D is idle; 1 = A/D is busy, must wait for completion

ADWAIT A/D circuit settling indicator: 0 = circuit is idle, conversion can start; 1 = circuit is busy, must wait

ADPOL A/D polarity configuration: 0 = Bipolar, 1 = Unipolar

ADSD A/D single-ended / differential configuration: 0 = Single-ended, 1 = Differential

16.2 Select the Input Channel

To select the input channel to read, write a low-channel/high-channel pair to the channel register at Base+2. The low four bits select the low channel, and the high four bits select the high channel. When you write any value to this register, the current A/D channel is set to the low channel.

For example, to program the board to sample channel 4 only, write 0x44 to Base+2. To program the board to sample channels 0 through 15 in sequence, write 0xF0 to Base+2.

When you perform an A/D conversion, the current channel automatically increments to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write 0x20 to base+2. The first conversion is on channel 0, the second will be on channel 1 and the third will be on channel 2. The channel counter wraps around to the beginning so the fourth conversion will be on channel 0 again.

```
outp(base+2, 0x22);     // example, set channel range to fixed channel 2
outp(base+2, 0x70);     // example, set channel range to 0-7
```

16.3 Select the Input Range

Select the input range from among the available options in the table in section 15.2. If the range is the same as for the previous A/D conversion it does not need to be set again. Write this value to the input range register at Base+3.

```
outp(base+3, 0x01);           // example: set gain = 2
```

16.4 Select the Polarity

Select the polarity from among the available options in the table in section 15.2. If the polarity is the same as for the previous A/D conversion it does not need to be set again. Write this setting along with the single-ended/differential setting to the register at page 2 base+13. To access page 2, the page must be set with the page register at base+1.

```
outp(base+1, 2);         // set page
outp(base+13, 0x00);     // example: sets bipolar, single-ended
outp(base+13, 0x08);     // example: sets unipolar, single-ended
```

16.5 Wait for Analog Input Circuit to Settle

After writing to either the channel register, Base+2, the input range register, Base+3, or the polarity register at page 2 base+13, you need to allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10µs timer to assist with the wait period. Monitor the WAIT bit at Base+3, bit 5. When the bit value is 1, the circuit is actively settling on the input signal. When the value is 0, the board is ready to perform A/D conversions. The below code will work but does not account for possible hardware problems which could cause the program to freeze. A better approach is to enable a timeout by using a loop that will exit after a fixed number of tests.

```
while (inp(base+3) & 0x20);   // wait for ADWAIT to go low, base+3 bit 5
```

16.6 Perform an A/D Conversion on the Current Channel

After the above steps are completed, start the A/D conversion by writing to the ADSTART bit at base+0. This write operation only triggers the A/D if AINTE = 0 (interrupts are disabled). When AINTE = 1, the A/D can only be triggered by the on-board counter/timer or an external signal. This protects against accidental triggering by software during a long-running interrupt-based acquisition process.

```
outp(base,0x80);
```

16.7 Wait for the Conversion to Finish

The A/D converter chip takes up to 5us to complete one A/D conversion. Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after starting the conversion, the read will occur before the A/D conversion completes and return invalid data. Therefore, the data acquisition circuit provides a status bit ADBUSY to indicate whether the A/D circuit is busy or idle. This bit can be read back from the status register at Base+3, bit 7. When the A/D converter is busy (performing an A/D conversion), ADBUSY=1 and the program must wait. When the A/D converter is idle (conversion is done and data is available), ADBUSY=0 and the program may read the data.

```
while (inp(base+3) & 0x80);   // wait for ADBUSY to go low, base+3 bit 7
```

The above example could hang your program if there is a hardware fault and the bit is stuck at 1. A better solution is to use a loop with a timeout, as shown below.

```
int checkstatus()                    // returns 0 if ok, -1 if error
{
int i;
for (i = 0; i < 20000; i++)
if (!(inp(base+3) & 0x80)) return(0);     // conversion completed
return(-1);                          // conversion did not complete
}
```

16.8 Read the Data from the Board

Once the conversion is complete, you can read the data back from the A/D converter. The data is a 16-bit value and is read back in two 8-bit bytes. The LSB must be read from the board before the MSB because the data is inserted into the board's FIFO in that order. Unlike other registers on the board, the A/D data may only be read one time, because each time an A/D sample is read from the FIFO, the internal FIFO pointer advances and that sample is no longer available. Reading data from an empty FIFO returns unpredictable results.

The following code illustrates how to read and construct the 16-bit A/D value.

```
LSB = inp(base);
MSB = inp(base+1);
ADdata = MSB * 256 + LSB;     // combine the 2 bytes into a 16-bit value
```

The final value is interpreted as a 16-bit signed integer in the range -32768 to +32767. This numerical value is then converted to a voltage depending on the selected input range as explained below.

In scan mode, the behavior is the same except when the program initiates a conversion, all channels in the programmed channel range will be sampled once and the data will be stored in the FIFO. The FIFO depth register increments by the scan size. When STS goes low, the program should read out the data for all channels.

16.9 Convert the Data to Volts or Engineering Units

Once the A/D value is read, it needs to be converted to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards, you may need to convert the voltage to some other engineering units. For example, the voltage may come from a temperature sensor and the voltage would then need to be converted to the corresponding temperature, according to the temperature sensor's characteristics.

Since there are many possible formulas for converting the input voltage to engineering values, this secondary step is not included here. Only conversion to input voltage is described. However, you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas.

16.9.1 Conversion Formula for Bipolar Input Ranges

Input voltage = A/D value / 32768 * Full-scale input voltage

Example:

For bipolar input range ±5V, full-scale input voltage = 5V

For an A/D value of 17761: Input voltage = 17761 / 32768 * 5V = 2.710V

For a bipolar input range, 1 LSB = 1/32768 * Full-scale voltage, in this case 5V/32768 = 153uV (0.000153V).

The table below shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage).

A/D Code	*Input Voltage Symbolic Formula*	*Input Voltage for ±5V Range*
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	V_{FS} - 1 LSB	4.9998V

16.9.2 Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D value + 32768) / 65536 * Full-scale input voltage

Example:

For unipolar input range 0-5V, full-scale input voltage = 5V.

For an A/D value of 17761: Input voltage = (17761 + 32768) / 65536 * 5V = 3.855V

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage, in this case 5V/65536 = 76uV (0.000076V).

The table below shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage).

A/D Code	*Input Voltage Symbolic Formula*	*Input Voltage for 0-5V Range*
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.000076V
...	...	...
-1	V_{FS} / 2 - 1 LSB	2.4999V
0	V_{FS} / 2	2.5000V
1	V_{FS} / 2 + 1 LSB	2.5001V
...	...	...
32767	V_{FS} - 1 LSB	4.9999V

17. A/D SCAN, INTERRUPT AND FIFO OPERATION

The control bits SCANEN (scan enable) and AINTE (A/D interrupt enable) in conjunction with the FIFO determine the behavior of the board during A/D conversions and interrupts.

FIFO Operation

A FIFO integrated into the FPGA design provides a temporary buffer for storing A/D conversions before the application program reads them. The main purpose of the FIFO is to reduce the interrupt rate in order to reduce the software load on the processor during high speed sampling.

On power-up or reset, the FIFO is set to basic mode, with depth 48 with threshold 16 for backward compatibility with older Diamond products. When EXFIFO=1 (expanded FIFO mode is set), the FIFO is set to depth 2048 with threshold 1024. At the end of an AD conversion, the 16-bit A/D data is latched into the FIFO. A/D Data is read out of the FIFO with 2 read operations, first Base + 0 (LSB) and then Base + 1 (MSB). The A/D FIFO depth register FDn:0 keeps track of the number of A/D samples in the FIFO. Each time an A/D conversion completes, data is written into the FIFO and the depth register increments by 1. When the MSB of the A/D data is read, the FIFO depth counter will decrement by 1 sample.

If the FIFO reaches its limit (48 samples in basic mode, 2048 samples in enhanced mode), then the next time an A/D conversion occurs the Overflow flag OF will be set. In this case the FIFO will not accept any more data, and its contents will be preserved and may be read out. In order to clear the overflow condition, the program must reset the FIFO by writing to the RSTFIFO bit in Base + 1, or a hardware reset must occur.

Scan operation

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range programmed in Base + 2. When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger. The total sample rate of the board is equal to the scan rate (A/D trigger rate) times the number of channels in the scan (scan size). The total sample rate cannot exceed the board's limit of 250KHz.

Interrupt operation

When AINTE=1 (base+4 bit 0), once the FIFO depth equals or exceeds the programmed depth value, an interrupt request will occur. If AINTE = 0, the FIFO threshold is ignored and the FIFO continues to fill up.

To detect if an interrupt has occurred, the AINT status bit can be read (base+7 bit 4). To clear the interrupt, write a 1 to the CLRA bit (base+0 bit 0) or disable analog interrupts by setting AINTE=0.

When an interrupt is pending, the IRQ line will be driven high. When no interrupt is pending, the board will release the IRQ line and it will be pulled low by the pull-down resistor configured with J21. It is possible for Helios to generate interrupts from up to 3 sources simultaneously. Thus clearing one interrupt will not necessarily cause the IRQ line to go low. It will only go low when all 3 circuits are inactive or have no interrupts pending.

In Scan mode (SCANEN = 1), the FIFO threshold should be set to a number at least equal to the scan size and in all cases equal to an integral number of scans. For example if the scan size is 8 channels, the FIFO threshold should be set to 8, 16, 24, 32, … but not less than 8. This way the interrupt will occur at the end of the scan, and the interrupt routine can read in a complete scan or set of scans each time it runs.

In non-scan mode (SCANEN = 0), the FIFO threshold should be set to a level that minimizes the interrupt rate but leaves enough time for the interrupt routine to respond before the FIFO fills up. No A/D data is available to the application program until the interrupt occurs, so if the threshold is high but the rate is slow, the delay to receive A/D data may be longer than acceptable. Therefore for slow sample rates the FIFO threshold should be small. If the sample rate is high, the FIFO threshold should be high to reduce the interrupt rate. However remember that the remaining space in the FIFO determines the time the interrupt routine has to respond to the interrupt request. If the FIFO threshold is too high, the FIFO may overflow before the interrupt routine responds. A good rule of thumb is to set the FIFO threshold so as to limit the interrupt rate to no more than 1,000-2,000 per second in Windows and Linux or 10,000 per second in DOS.

Here are some general guidelines for FIFO thresholds. Experimentation may be necessary to determine the optimum FIFO threshold for each application. Total sample rate means sample rate for sample (non-scan) mode and scan rate times scan size for scan mode. In general, the FIFO should always be used in enhanced mode unless the sample rate is very slow and you want to have a very low FIFO threshold to receive interrupts on every sample or every scan.

If total sample rate is:	**Set FIFO threshold to (non-scan):**	**Set FIFO threshold to (scan):**
0 to 100Hz	1	scan size
>100Hz up to 1KHz	1 – 10	1 – 10 times scan size
>1KHz up to 10KHz	10 – 100	10 – 100 times scan size
>10KHz up to 100KHz	512 – 1500	Multiple of scan size within range 512-1500

Function Modes

The table below describes the board's behavior for each of the 4 possible cases of AINTE and SCANEN (interrupt operation and scan operation). The interrupt software behavior given in the table describes the operation of the Diamond Systems Universal Driver software. If you write your own software or interrupt routine you should conform to the described behavior for optimum results.

AINTE Base+4 bit 0	***SCANEN Base+2 bit 1***	***Operation***
0	0	**Software-triggered A/D samples** Single A/D conversions are triggered by write to ADSTART bit at base+0. ADBUSY stays high during the A/D conversion. No interrupt occurs. The user program monitors ADBUSY (Base+3, bit 7) and reads A/D data when ADBUSY goes low.
0	1	**Software-triggered A/D scans** A/D scans are triggered by write to ADSTART bit at base+0. All channels between LOW and HIGH are sampled once on each scan. ADBUSY stays high during the entire scan (multiple A/D conversions). No interrupt occurs. The user program monitors ADBUSY (Base+3, bit 7) and reads A/D data for all channels when ADBUSY goes low.
1	0	**Clock-triggered A/D samples with interrupts** Single A/D conversions are triggered by the source selected with ADCLK (Base+4, bit 4). ADBUSY stays high during the A/D conversion. A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads the number of samples equal to the programmed FIFO threshold.
1	1	**Clock-triggered A/D scans with interrupts** A/D scans are triggered by the source selected with ADCLK (Base+4, bit 4). ADBUSY stays high during the entire scan (multiple A/D conversions). A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads the number of samples equal to the programmed FIFO threshold.

18. DIGITAL-TO-ANALOG OUTPUT RANGES AND RESOLUTION

18.1 Description

Helios uses a 4-channel D/A converter (DAC) to provide four analog voltage outputs. The standard configuration uses a 12-bit DAC, however a 16-bit DAC is available as a special ordering option. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that the DAC supports is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve with a 12-bit number.

18.2 D/A Resolution

The resolution is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full range of possible output voltages, called the full scale range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 least significant bit (1 LSB). The value of this LSB is calculated as follows:

12-bit DAC: 1 LSB = Full scale range / 4096

16-bit DAC: 1 LSB = Full scale range / 65536

Example for 12-bit DAC:

For output range = unipolar 0-10V, Full scale range = 10V – 0V = 10V, so 1 LSB = 10V / 4096 = 2.44mV.

For output range = bipolar ±10V, Full scale range = 10V – (-10V) = 20V, so 1 LSB = 20V / 4096 = 4.88mV.

18.3 Output Range Selection

The D/A output range is determined by the values of the register bits DAPOL, DAG!, and DAG0 in the register at page 2 base+14. When a value is written to this register, the D/A range for the selected channel will be set to the selected value. Each D/A channel can have its own range. To set all channels to the same range, set bit DAUR=0 when selecting the output range. To set a channel to its own range, set DAUR=1 and then select the channel using bits DACH1-0.

DAPOL	DAG1	DAG0	DAC output range or function
0	0	0	0 to 5V (unipolar 5V span)
1	0	0	±2.5V (bipolar 5V span)
0	0	1	0 to 10V (unipolar 10V span)
1	0	1	±5V (bipolar 10V span)
0	1	0	Not Used – Setting Ignored
1	1	0	±10V (bipolar 20V span)
X	1	1	D/A converter shut down

18.4 D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages. The D/A code is always an integer. For a 12-bit D/A (Standard models of Helios), the D/A code ranges between 0 and 4095 (2^{12}-1). For a 16-bit D/A (custom option), the D/A code ranges between 0 and 65535 (2^{16}-1).

18.4.1 D/A Conversion Formulas for Unipolar Output Ranges

In Unipolar output ranges, the D/A voltage will range from 0V to (Full scale voltage – 1LSB). Thus the full scale range is the same as the full scale voltage.

12-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 4096

Output voltage = (D/A code / 4096) * Full scale voltage

1 D/A LSB = Full scale voltage / 4096

16-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 65536

Output voltage = (D/A code / 65536) * Full scale voltage

1 D/A LSB = Full scale voltage / 65536

Example for 12-bit D/A:

Output range is unipolar 0 – 10V (full scale voltage = full scale range = 10V); Desired output voltage = 2.000V.

D/A code = 2.000V / 10V * 4096 = 819.2 => 819

1 LSB = 10V / 4096 = 2.44mV

The following table illustrates the relationship between D/A code and output voltage for a unipolar output range (VREF = Reference voltage).

12-Bit D/A Code	*Output Voltage Symbolic Formula*	*Output Voltage for 0-10V Range*
0	0V	0.0000V
1	1 LSB (V_{REF} / 4096)	0.0024V
...	...	...
2047	V_{REF} / 2 - 1 LSB	4.9976V
2048	V_{REF} / 2	5.0000V
2049	V_{REF} / 2 + 1 LSB	5.0024V
...	...	...
4095	V_{REF} - 1 LSB	9.9976V

18.4.2 D/A Conversion Formulas for Bipolar Output Ranges

In Bipolar output ranges, the D/A voltage will range from (– full scale voltage) to (+ full scale voltage - 1LSB). Thus the full scale range is 2x the full scale voltage.

12-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 2048 + 2048

Output voltage = ((D/A code – 2048) / 2048) * Full scale voltage

1 LSB = Full scale voltage / 2048, or 1 LSB = Full scale output range / 4096

16-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 32768 + 32768

Output voltage = ((D/A code – 32768) / 32768) * Full scale voltage

1 LSB = Full scale voltage / 32768, or 1 LSB = Full scale output range / 65536

Example for 12-bit D/A:

Output range is bipolar ±10V (full scale voltage = 10V, full scale range = 20V); desired output voltage = 2.000V.

D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

1 LSB = 10V / 2048 = 4.88mV

The D/A code should be rounded to the nearest integer for best accuracy.

The following table illustrates the relationship between D/A code and output voltage for a bipolar output range (VREF = Reference voltage).

12-Bit D/A Code	*Output Voltage Symbolic Formula*	*Output Voltage for ±10V Range*
0	$-V_{REF}$	-10.0000V
1	V_{REF} + 1 LSB	-9.9951V
...	...	...
2047	-1 LSB	-0.0049V
2048	0	0.0000V
2049	+1 LSB	0.0049V
...	...	...
4095	V_{REF} - 1 LSB	9.9951V

19. GENERATING AN ANALOG OUTPUT

There are 5 steps involved in performing a D/A conversion, or generating an analog output. Each step is described in more detail below. These instructions describe the necessary steps. The examples provided use direct programming instead of Universal Driver software for illustration. For instructions on generating an analog output using the Universal Driver, refer to the software user manual.

1. Set simultaneous update mode and/or DAC resolution if needed.
2. Configure the desired output range.
3. Compute the D/A code for the desired output voltage.
4. Write the value to the selected output channel.
5. Update the D/A.

Base +	R/W	7	6	5	4	3	2	1	0
Main Registers									
1	W	-	-	-	-	-	-	PG1	PG0
6	W	**DA7**	**DA6**	**DA5**	**DA4**	**DA3**	**DA2**	**DA1**	**DA0**
7	W	**DACH1**	**DACH0**	-	-	**DA11**	**DA10**	**DA9**	**DA8**
11	R/W	DIOCTR	**DAMODE**	**DASIM**	DIRA	DIRCH	-	DIRB	DIRCL
Page 2: Expanded FIFO and AD/DA Control									
14	W	**DAUR**	-	**DARCH1**	**DARCH0**	**DAPOL**	-	**DAG1**	**DAG0**
15	W	**DA15**	**DA14**	**DA13**	**DA12**	**DA11**	**DA10**	**DA9**	**DA8**
15	R	-	-	-	-	-	-	-	-

DA7-0 D/A data bits 7-0 for both 12-bit and 16-bit modes. DA0 is the LSB

DA11-0 (in base+7) D/A data bits 11-8 for 12-bit mode only; DA11 is the MSB

DA15–8 (in page 2 base+15) D/A data bits 15 – 8 for 16-bit mode only; DA15 is the MSB

DACH1-0 D/A channel to receive current data in DA11-0 or DA15-0

DAMODE 16/12-bit DAC mode. This bit should only be set for custom models of Helios with a 16-bit DAC

DASIM D/A simultaneous mode: 0 = immediate update with new data, 1 = simultaneous mode

DAUR D/A unique range: 1 = set selected channel to given range, 0 = set all channels to same range

DARCH1-0 D/A channel to configure for given range when DAUR = 1

DAPOL D/A polarity setting: 0 = unipolar, 1 = bipolar

DAG1-0 D/A gain setting

DACBSY Indicates the DAC is busy updating (approx. 4 µS). 1 = Busy, 0 = Idle. Any writes to the DAC (registers 6 and 7 of page 0 or register 15 of page 2) while DACBSY = 1 will be ignored.

19.1 Set Simultaneous Update Mode and/or DAC Resolution

If simultaneous update is desired, the DASIM bit should be set **before** writing the data to the DAC so that it will not update immediately. Then after all new DAC data is written, the DAC update can be initiated. The DASIM remains in effect until it is changed or a board or system reset occurs.

```
outp(base+11, inp(base+11) | 0x20); // set bit 5 for simultaneous update
outp(base+11, inp(base+11) & 0xDF); // clear bit 5 for individual update
```

The standard model of Helios uses a 12-bit DAC, and no resolution setting is required. If a 16-bit DAC is installed in a custom configuration of Helios, the DAMODE bit must be set to tell the FPGA where the DAC MSB data is found when loading the DAC. The DAMODE bit only needs to be set one time at the start of the program.

```
outp(base+11, inp(base+11) | 0x40); // set bit 6 for 16-bit DAC
```

19.2 Configure the Desired Output Range

Helios features programmable D/A output ranges. You can set one range for all 4 channels or set individual output ranges for each channel. The output range is set with register bits DAPOL and DAG1-0. See the table in section 18.3 on page 40 to select the bit values needed for the desired output range.

To set all 4 channels to the same output range, simply write the desired values of DAPOL and DAG1-0 to the register at page 2 base+14, leaving all other bits at 0. To set an individual range, set DAUR=1 and select the channel with DAGCH1-0 in this register at the same time as you write the DAPOL and DAG1-0 bits.

To set all channels to the same output range:

```
outp(base+1, 2);  // select page 2
outp(base+14, (DAPOL << 3) + gain); // gain = 0, 1, 2, or 3 as appropriate
```

To set a channel to a unique output range:

```
outp(base+1, 2);  // select page 2
value = 0x80 + (DACH << 4) + (DAPOL << 3) + gain;     // DACH = D/A channel
0-3
outp(base+14, value);   // sets individual D/A channel to desired range
```

19.3 Compute the D/A Code for the Desired Output Voltage

Use the formulas in chapter 18 to compute the D/A code required to generate the desired voltage.

19.4 Write the Value to the Selected Output Channel Registers

Use the following formulas to compute the LSB and MSB values from the D/A code. The calculation is the same for both 12-bit and 16-bit DAC.

LSB = D/A Code & 255 (keep only the low 8 bits)

MSB = int(D/A code / 256) (strip off low 8 bits, keep remaining bits)

The LSB is an 8-bit number in the range 0-255. For a 12-bit DAC, the MSB is a 4-bit number in the range 0-15, while for a 16-bit DAC the MSB is an 8-bit number in the range 0-255. The MSB is always rounded *down*. The truncated portion is accounted for by the LSB.

Example:

Output code = 1776

LSB = 1776 & 255 = **240** (0xF0)

MSB = int(1776 / 256) = int(6.9375) = **6** (always round down!)

The LSB is written to Base+6. For the 12-bit DAC, the MSB and channel number are written to base+7 (MSB = bits 0-3, channel number 0-3 = bits 6-7). For the 16-bit DAC, the MSB is written to page 2 base+14, and the channel is written separately to base+7. Accessing page 2 requires setting the page register in base+1. In addition, for a 16-bit DAC, the DAMODE bit must be set to configure the circuit for 16-bit data values.

Example for 12-bit DAC:

```
outp(base+6, LSB);
outp(base+7, MSB + (channel << 6));
```

Example for 16-bit DAC:

```
outp(base+6, LSB);
outp(base+1, 2);              // select page 2
outp(base+15, MSB);           // write MSB to the MSB register in page 2
outp(base+7, channel << 6);   // channel no. still goes in base+7 bits 7-6
```

19.5 Update the D/A

The DASIM bit (base+11 bit 5) determines when the D/A will be updated. If the D/A is not set up for simultaneous operation (DASIM=0), then writing the channel number to base+7 will automatically update the selected D/A channel with the new data. The update takes approximately 4uS to complete. No writes should occur to the DAC while an update is in progress. While the update is occurring, the DACBSY bit in base+3 bit 4 will be 1. You can monitor this bit to wait for the update to finish if there is a possibility that your application will attempt to access the DAC before the update completes. To prevent software from hanging due to a hardware error, a timeout should be built into the checking.

```
// this will exit if DACBSY = 0 or loop reaches terminal count
for (i=0; i<100000; i++) if (inp(base+3) & 0x10 == 0) break;
```

If DASIM=1, the DAC is set up for simultaneous mode, meaning that an update will only occur when a specific update command is issued to the DAC. This lets you preload multiple channels with new data and then update them all at the same time. First load data into the DACs in the standard manner as described above, then issue the update command by reading from page 2 base+15. The value read has no meaning and should be ignored.

Note that the simultaneous update command always updates all 4 channels. Any channel with new data will change to reflect the new data. Any channel which has not been changed since it was last updated will simply reload the same value and therefore will remain steady.

```
outp(base+1, 2);        // select page 2
a = inp(base+15);       // read register to update all DACs
```

20. ANALOG CIRCUIT CALIBRATION

The Helios data acquisition circuit contains an advanced autocalibration circuit that can maintain the accuracy of both A/D and D/A circuits to within the specified tolerances regardless of time and temperature. Autocalibration is supported in the Diamond Systems Universal Driver software included with the board.

The autocalibration circuit uses an ultra-stable +5V reference voltage IC as the source for its calibration. Both A/D and D/A circuits are calibrated in the analog domain by using a series of 8-bit “TrimDACs” to adjust the offset and gain settings of the circuits. The data values driving the DACs are stored in an EEPROM and are loaded automatically each time the board powers up.

During the autocalibration process, the board will measure the on-board reference and calibrate the A/D circuit by adjusting the TrimDACs to achieve the best accuracy. Once the A/D circuit is calibrated, the D/A circuit is calibrated by routing the D/A outputs into the A/D converter and adjusting them as well. The new calibration values for the TrimDACs are stored back into the EEPROM so they can be automatically recalled thereafter.

A unique feature of Diamond’s autocalibration process is that each analog input range is individually calibrated for optimum performance. Analog amplifier circuits with 16-bit accuracy exhibit gain and offset errors that vary depending on the gain setting. The settings that work best for one range may not be sufficient to calibrate another. If a circuit is calibrated for maximum accuracy in a particular input range, such as +/-5V, changing the input range to +/-10V or 0-2.5V may introduce errors that exceed the resolution of a 16-bit measurement and will require calibration again.

To counteract this phenomenon, Diamond’s autocalibration circuit provides for a separate complete set of calibration settings for each analog input range. During the autocalibration process, each range is calibrated one at a time, and its set of calibration settings is stored in a separate area of the EEPROM’s memory. One of these ranges is identified as the “boot range”, and this range’s calibration values are the ones that are automatically recalled during power-up. You have the option of specifying the boot range, which should be chosen as the range most commonly used in your application. When you change the input range, you have the option of loading the calibration values for the new input range to maintain optimum accuracy of your measurements.

The autocalibration process is triggered with a single function call in the Diamond Universal Driver software. The process takes about 10-20 seconds to calibrate the complete set of analog input ranges and about the same time for the D/A circuit. Autocalibration can easily be incorporated into your application program, so that you can calibrate the data acquisition circuit as often as necessary while your system is running.

21. DIGITAL I/O PORTS

Helios has two groups of digital I/O ports and one digital interrupt circuit:

- 3 8-bit ports named A, B, and C are included in the data acquisition circuit on the AV model and are available on connector J17 on that model.
- 2 8-bit ports named D and E are provided by the digital I/O circuit integrated into the Vortex processor and are available on connector J7 on all models.
- An interrupt on the ISA bus may be triggered using the EXTTRIG pin on connector J17 on the AV model.

21.1 Data Acquisition Circuit Digital I/O Ports

These 3 ports are called A, B, and C and are accessible on the data acquisition I/O connector J17. Ports A and B can be configured as either input or output, and each half of port C can be configured independently for input or output. The data is read and written with the registers at base+8 through base+10, and the direction configuration byte is located at register Base+11. See the detailed register description in chapter 14 on page 46.

To use these ports, first configure the desired directions by writing the appropriate configuration value to base+11. Then read or write data to the 3 I/O ports as needed. All I/O ports are in input mode on power-up or after a board reset.

The upper 4 bits of port C serve dual purposes. If control bit DIOCTR=0, these bits are normal DIO lines and can be read or written via the register at base+10. If DIOCTR=1, these bits are reassigned as counter/timer signals:

J17 Pin No.	DIOCTR = 1	DIOCTR = 0
21	Gate 0	DIO C4
22	Gate 1	DIO C5
23	Clk 1	DIO C6
24	Out 0	DIO C7

Register Map for Data Acquisition Circuit Digital I/O Ports:

Base +	R/W	7	6	5	4	3	2	1	0
8	R/W	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
9	R/W	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
10	R/W	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
11	R/W	**DIOCTR**	DAMODE	DASIM	**DIRA**	**DIRCH**	-	**DIRB**	**DIRCL**

A7-0	Digital I/O port A
B7-0	Digital I/O port B
C7-0	Digital I/O port C, split into two 4-bit halves
DIOCTR	Se description above and chapter 22 for DIOCTR's effect on I/O connector J17
DIRA	Port A direction. 0 = output, 1 = input
DIRB	Port B direction: 0 = output, 1 = input
DIRCH	Port C bits 7-4 direction: 0 = output, 1 = input. This bit has no effect if DIOCTR=1.
DIRCL	Port C bits 3-0 direction: 0 = output, 1 = input

21.2 Vortex Processor Digital I/O Ports

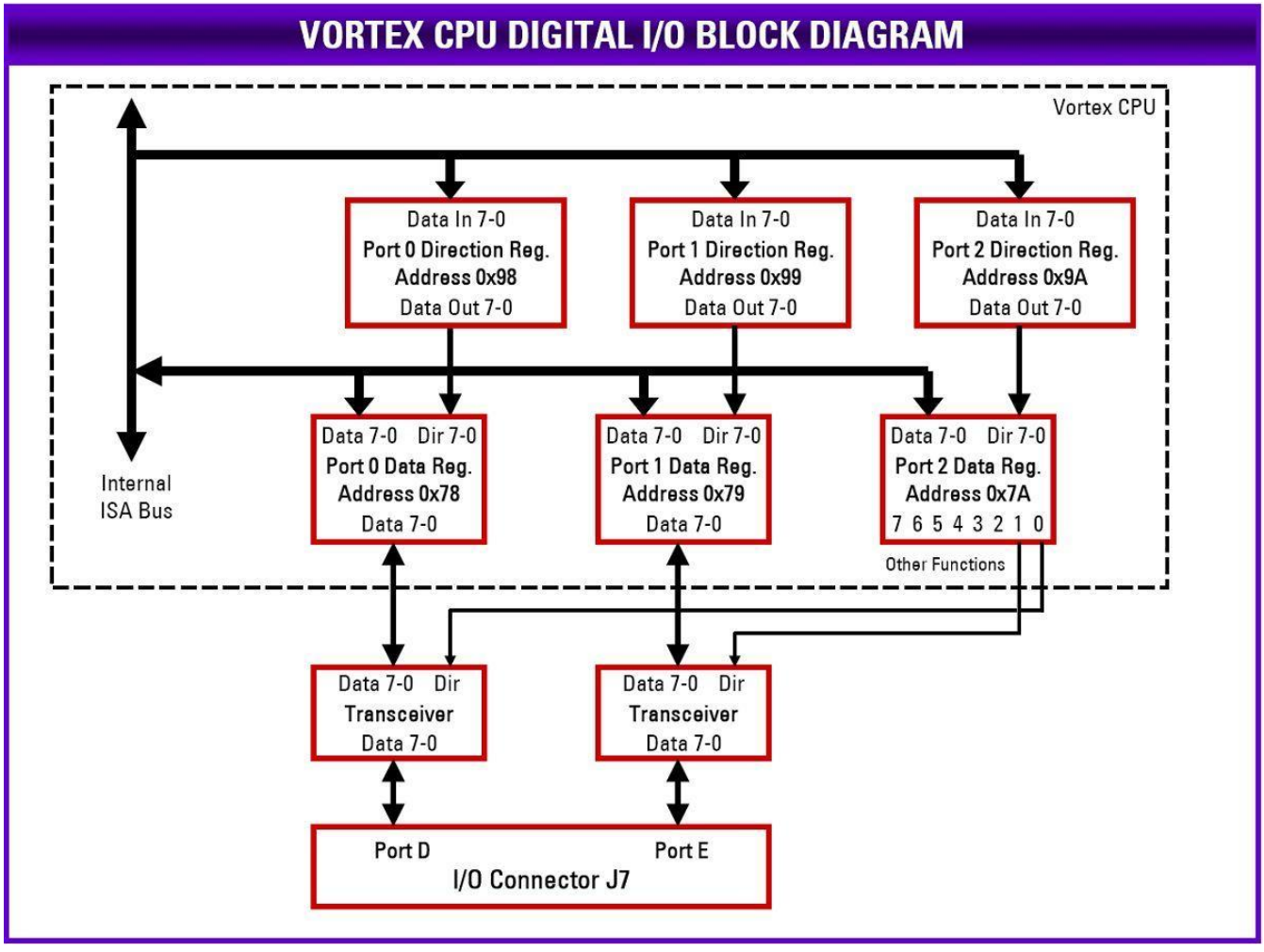
The Vortex processor has an integrated digital I/O (GPIO) circuit with 5 8-bit ports. Two of them (ports 0 and 1) are available for use as general purpose digital I/O on Helios and are identified as ports D and E. These ports are accessible on I/O connector J7. The other 3 ports (2, 3, and 4) are reserved for other functions and should not be disturbed except as described in this manual. All GPIO ports are addressable in the ISA bus I/O space.

Each GPIO port has a data register and a direction register. Before the port can be used, the direction register must be configured. Each port is isolated from the I/O connector via an 8-bit bi-directional transceiver to protect the processor chip and provide enhanced output current capability. These transceivers require all 8 bits to be the same direction. Therefore each GPIO port direction register must be configured as either all input or all output.

The two 8-bit transceivers must also have their direction configured to match the intended direction of the two GPIO ports. To avoid possible conflicts in the circuitry with the processor and the transceiver driving their data lines simultaneously, the first step is to configure the direction of the transceivers.

The I/O addresses of the GPIO data and direction ports are as follows:

Vortex GPIO Port	*Helios Function*	*Data Register*	*Direction Register*
0	Port D / GPIO port 0	0x78	0x98
1	Port E / GPIO port 1	0x79	0x99
2	Ports D/E direction control	0x7A	0x9A



Direction Control Register

The GPIO port 2 direction register at address 0x9A should always be set for all output mode by writing 0xFF to it. This is the default setting, so no change should be required. Then the DIO port D/E direction control data can be written to bits 1 and 0 of address 0x7A. Bit 1 controls the direction for port E, and bit 0 controls the direction for port D. A 1 sets the port for output, and a 0 sets the port for input.

The data written to the direction control register should be confined to bits 1 and 0, because the other bits are used for the serial port 1 and 2 protocol selection and should not be disturbed. The bits are set by first reading the current register value, modifying the selected bit or bits, and then rewriting the data to the port. The example C code below shows how to do this:

```
dir = inp(0x7A);  // read current port 2 register data
dir &= 0xFE;      // example, clear bit 0 to configure port D as input
dir |= 2;         // example, set bit 1 to configure port E as output
outp(0x7A, dir);  // write new data to port 2 register
```

Port Direction Registers

To set a port to output, first set the corresponding port 2 direction bit at address 0x7A to 1, then set the port 0 direction register 0x98 or port 1 direction register 0x99 to 0xFF.

To set a port to input, first set the port 0 direction register 0x98 or port 1 direction register 0x99 to 0x00, then set the corresponding direction bit at port 2 / address 0x7A to 0.

The only valid values for the port 0/1 direction registers are FF and 00, since all bits in the port must be set to the same direction due to the presence of the transceiver chip between the port and the I/O connector. The sequences above are important to avoid conflicts with both the CPU chip and the transceiver chip driving their connection simultaneously.

Port Data Registers

Once the direction registers for ports D and E are configured, the ports can be read or written as required at addresses 0x78 and 0x79. Reading a port set for input mode will return the data on the corresponding I/O connector pins. Writing a port in input mode will have no effect. Reading a port in output mode will return the value last written into that port. Writing a port in output mode will send that data to the corresponding I/O connector pins.

The example C code below shows how to configure and use ports D and E. In this code the example configuration above is assumed to have already been executed, namely port D = input and port E = output.

```
outp(0x98, 0);          // set port D to input
outp(0x99, 0xFF);       // set port E to output
ddata = inp(0x78);      // read data from port D
edata = 0x12;           // set port E to 00010010
outp(0x79, edata);      // write new data to port E
```

21.3 Digital Interrupts

The data acquisition circuit on the AV model can generate interrupts on the ISA bus when a rising edge occurs on the EXTTRIG pin (J17 pin 25). This pin is pulled high when unconnected. The interrupt occurs on the IRQ level configured with jumper block J21. To enable digital interrupts, set bit DINTE=1 (base+4 bit 1). To generate an interrupt, drive pin 25 low and then high again (or release it to open circuit). To detect if an interrupt has occurred, read the DINT status bit (base+7 bit 5). A 1 = interrupt pending, 0 = no interrupt pending. To clear the interrupt request, write a 1 to the CLRD bit (base+0 bit 1) or disable digital interrupts by setting DINTE=0.

When an interrupt is pending, the IRQ line will be driven high. When no interrupt is pending, the board will release the IRQ line and it will be pulled low by the pull-down resistor configured with J21. It is possible for Helios to generate interrupts from up to 3 sources simultaneously. Thus clearing one interrupt will not necessarily cause the IRQ line to go low. It will only go low when all 3 circuits are inactive or have no interrupts pending.

22. COUNTER/TIMER OPERATION

The AV model of Helios with data acquisition contains two counter/timers that provide various timing functions on the board for A/D timing and user applications. These counters are controlled with registers in the on-board data acquisition controller FPGA. Base+4 includes counter configuration bits, and base+11 contains the configuration bit DIOCTR, which controls 4 dual-function I/O pins on the data acquisition connector J17.

Register Map for Counter/Timer Circuit

Page 0: Counter/Timer Access								
12	CtrD7	CtrD6	CtrD5	CtrD4	CtrD3	CtrD2	CtrD1	CtrD0
13	CtrD15	CtrD14	CtrD13	CtrD12	CtrD11	CtrD10	CtrD9	CtrD8
14	CtrD23	CtrD22	CtrD21	CtrD20	CtrD19	CtrD18	CtrD17	CtrD16
15	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

CTRD23-0 24-bit divisor or latch value for Counter 0

CTRD15-0 16-bit divisor or latch value for Counter 1

CTRNO Counter no. for command, 0 or 1

LATCH Latch the selected counter so that its value may be read. The counter must be latched before it is read. Reading from registers at page 0, base+12 thru base+14 returns the most recently latched or loaded value. If you are reading the 16-bit Counter 1 data, read only page 0, base+12 and base+13. Any data in page 0, base+14 will be from the previous 24-bit Counter 0 operation.

GTDIS Disable external gating for the selected counter (see GTEN below).

GTEN Enable external gating for the selected counter. If enabled, the associated J17 connector input signal GATE0 or GATE1 controls counting on the counter. If the GATEn signal is high, counting is enabled. If the GATEn signal is low, counting is disabled.

CTDIS Disable counting on the selected counter. The counter will ignore input pulses.

CTEN Enable counting on the selected counter. The counter will decrement on each input pulse.

LOAD Load the selected counter with the data written to page 0, base+12 through base+14 (Counter 0) or page 0, base+12 and base+13 (Counter 1).

CLR Clear the current counter (set its value to 0). Counter operation such as count enable or gate enable is not affected by the CLR command. If the counter is enabled it will continue to count input pulses.

22.1 Counter 0 – A/D Sample Rate Control

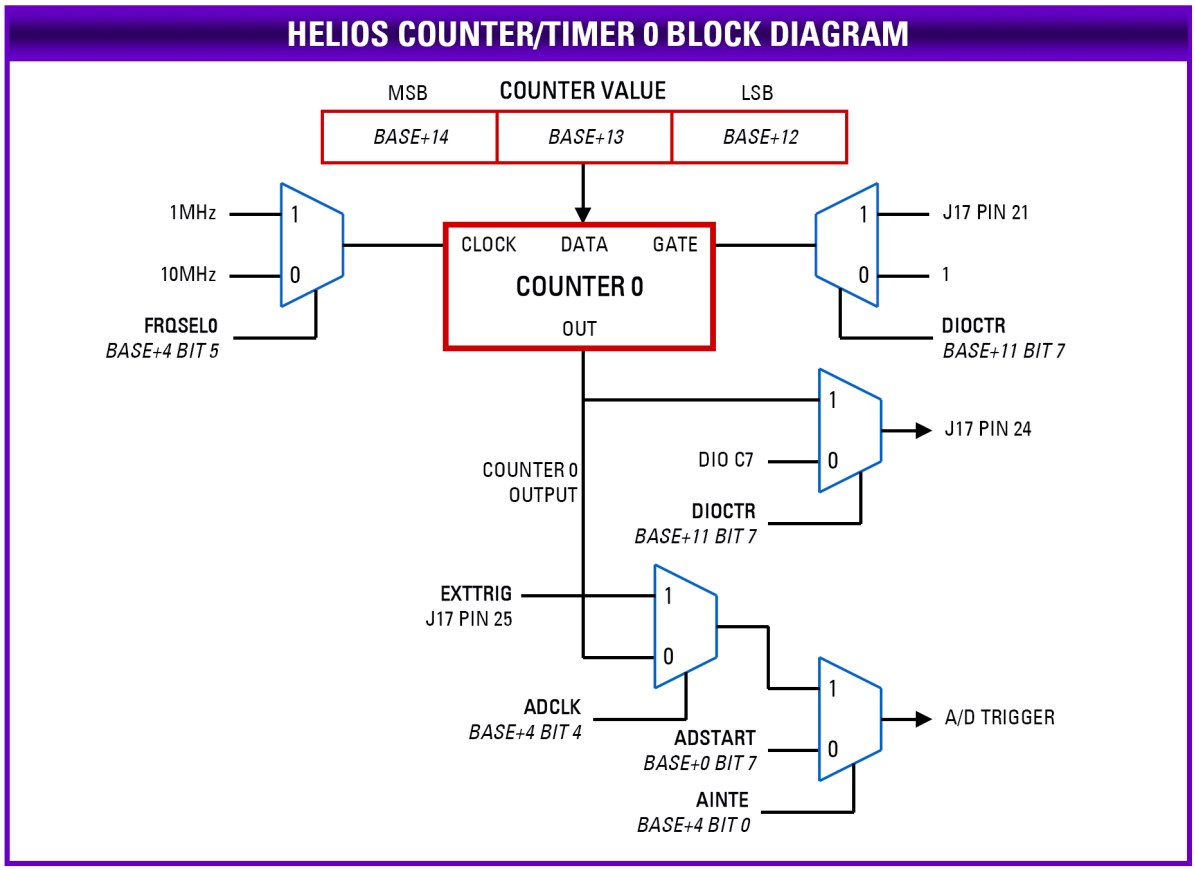
Counter 0 is a 24-bit, “divide-by-n” counter used for controlling the A/D sampling rate. The counter has a clock input, a gate input, and an output. The input is a 10MHz or 1MHz clock provided on the board and selected with bit CKFRQ0 in register Base+4, bit 5. The gate is an optional signal that can be input on pin 21 of I/O header J17 when DIOCTR (Base+11, bit 7) is 1. If DIOCTR=0, the counter runs freely. The output is a positive pulse whose frequency is equal to the input clock divided by the 24-bit divisor programmed into the counter. The output appears on pin 24 of the I/O header when DIOCTR is 1. If DIOCTR=0, the output is not accessible except as an A/D trigger.

The counter operates by counting down from the programmed divisor value. When the counter reaches a count of 1, it outputs a positive-going pulse equal to one input clock period (100ns or 1µs, depending on the input clock selected by FRQSEL0). On the next input clock, the counter then reloads to the initial load value and repeats the process indefinitely as long as it is enabled.

When AINTE=1 and ADCLK=0, the output can be used to trigger A/D conversions. If SCANEN=0, scan mode is disabled, and each clock pulse will cause the circuit to sample one A/D channel within the selected channel range. If SCANEN=1, scan mode is enabled, and each clock pulse will cause the circuit to sample each A/D channel within the selected channel range in quick succession.

The output frequency of counter 0 can range from 5MHz (10MHz clock, divisor = 2) to 0.06Hz (1MHz clock divided by 16,777,215, or 2^{24}-1).The fastest speed supported by the A/D circuit is 100KHz, so the counter should not be programmed to generate pulses faster than 100KHz when in non-scan mode and 100KHz divided by the size of the scan range when in scan mode.

The control register at page 0 Base+15 is used to load and clear the counter and to enable and disable counting. The optional gate (when DIOCTR=1) can be enabled and disabled, and the counter value can be latched for reading.



22.2 Counter 1 – Counting, Totalizing, and Interrupt Functions

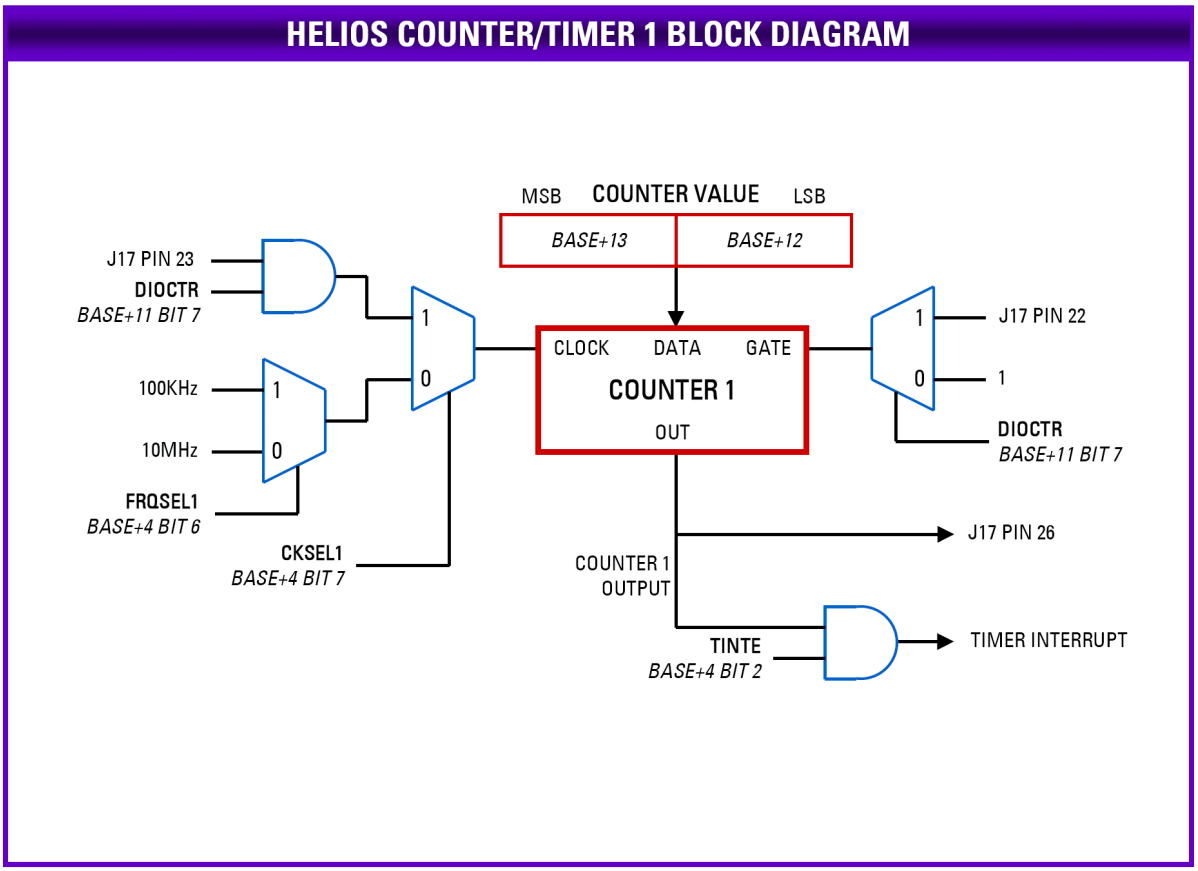
Counter 1 is similar to Counter 0 except that it is a 16-bit counter, and its clock, gate, and out connections have different options. The counter operates by counting down from the programmed divisor value. When the counter reaches a count of 1, it outputs a positive-going pulse equal to one input clock period. On the next input clock, the pulse terminates, and the counter reloads to the initial load value and repeats the process indefinitely as long as it is enabled. The output signal is available on I/O connector J17 pin 26.

When CKSEL1=0 in base+4, Counter 1 takes its input from the on-board clock source selected by FRQSEL1. When CKSEL1=1, counter 1 counts positive edges on data acquisition connector J17 pin 23, and DIOCTR in base+11 must also be set to 1 to configure this pin as an external clock input. This pin has a pull-up resistor, so the counter will not count if the pin is unconnected. **For proper operation, the input signal must be no greater than 10MHz, with both high and low periods of the cycle a minimum of 50ns in duration.**

When DIOCTR=1, the counter gate function is provided on pin 22 of the connector. If the gate is high, the counter counts, and if the gate is low, the counter holds its value and ignores input pulses. This pin has a pull-up resistor, so the counter can operate without any external gate signal attached. When DIOCTR=0, there is no gating, and the counter runs continuously when enabled.

Timer Interrupts

When TINTE=1 (base+4 bit 2), the output of timer 1 can be used to generate interrupts on the ISA bus at a user-programmable rate. The interrupt occurs on the IRQ level selected with jumper block J21. When an interrupt occurs, status bit TINT=1 (base+7 bit 6). The interrupt routine must clear the interrupt by driving bit CLRT=1 (base+0 bit 2) before terminating. When an interrupt is pending, the IRQ line will be driven high. When no interrupt is pending, the board will release the IRQ line and it will be pulled low by the pull-down resistor configured with J21. It is possible for Helios to generate interrupts from up to 3 sources simultaneously. Thus clearing one interrupt will not necessarily cause the IRQ line to go low. It will only go low when all 3 circuits are inactive or have no interrupts pending.



22.3 Command Sequences

Diamond Systems provides free Universal Driver software to control the counter/timers on Helios. The information in this section is intended as a guide for programmers writing their own code, instead of using the driver, and to give a better understanding of the counter/timer operation.

The counter/timer registers are located at page 0, base+1 through base+15. Be sure to select the correct page by writing to the PG1-0 bits in base+1.

Load and Enable a Counter

9. Write the data to the counter.

For counter 0, three bytes are required to load a 24-bit value. For counter 1, two bytes are needed for a 16-bit value. The value is an unsigned integer. Break the load value into 3 bytes: low, middle, and high, (Two bytes for Counter 1) and write the bytes to the data registers in any sequence.

Counter 0:

```
outp(base+12,low);
outp(base+13,middle);
outp(base+14,high);
```

Counter 1:

```
outp(base+12,low);
outp(base+13,high);
```

10. Load the counter.

```
outp(base+15,0x02);
```

```
outp(base+15,0x82);
```

11. Enable the counter gate if desired.

The gating may be enabled or disabled at any time. When gating is disabled, the counter counts all incoming edges. When gating is enabled, if the gate is high the counter counts all incoming edges and, if the gate is low, the counter ignores incoming clock edges.

```
outp(base+15,0x10);
```

```
outp(base+15,0x90);
```

12. Enable the counter.

A counter may be enabled or disabled at any time. If disabled, the counter ignores incoming clock edges.

```
outp(base+15,0x04);
```

```
outp(base+15,0x84);
```

Read a Counter

1. Latch the counter.

Counter 0:

```
outp(base+15,0x40);
```

Counter 1:

```
outp(base+15,0xC0);
```

2. Read the data.

The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

```
low=inp(base+12);
middle=inp(base+13);
high=inp(base+14);
```

```
low=inp(base+12);
high=inp(base+13);
```

3. Assemble the bytes into the complete counter value.

```
val = high*65536 + middle*256 + low;
```

```
val = high * 256 + low;
```

Disable the Counter Gate

Disabling the counter gate, as shown below, causes the counter to run continuously.

Counter 0:

```
outp(base+15,0x20);
```

Counter 1:

```
outp(base+15,0xA0);
```

Clear a Counter

Clear a counter to restart an operation. Normally, a counter is only cleared after stopping (disabling) and reading the counter. If you clear a counter while it is enabled, it continues to count incoming pulses so the counter value may not remain at zero.

1. Stop (disable) the counter.

```
outp(base+15,0x08);
```

```
outp(base+15,0x88);
```

2. Read the data (optional).

The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

```
low=inp(base+12);
middle=inp(base+13);
high=inp(base+14);
```

```
low=inp(base+12);
high=inp(base+13);
```

3. Clear the counter.

```
outp(base+15,0x01);
```

```
outp(base+15,0x81);
```

23. WATCHDOG TIMER

The watchdog timer can be used to trigger an interrupt or system reset upon the expiration of a programmed time interval. The purpose of this timer is to enable the system to recover from a software or hardware error that causes the system to freeze or get caught up in a software infinite loop.

The watchdog timer uses I/O address range 0x67 – 0x6D. It uses a 24-bit down counter for the timeout interval, with a resolution of 30.5usec. The shortest timeout interval is 30.5us, and the longest timeout interval is 30.5us x 2^{24} = 511 sec.

To use the watchdog timer, first make sure it is enabled in the BIOS. The default setting is enabled. Go to **Chipset** then **South Bridge Configuration** and select **Watchdog Configuration**. Set WDT1 to Enabled.

Once WDT1 is enabled, the steps are as follows: First program the desired timeout interval, then select the timeout event, then enable the timer. Once the timer is enabled, the software must reset it before it times out, or else the timeout event will occur. This reset must occur repeatedly until the watchdog timer is disabled.

The steps to set up and use the watchdog timer are as follows:

1. Write the desired time delay into registers 0x6A – 0x6C (0x6A is the LSB).
2. Select timer reset event using register 0x69.
3. Set register 0x68 bit 6 (0x40) to enable the timer.
4. To retrigger the timer and prevent the selected event from occurring, write any value to register 0x67 before the timer reaches zero. This procedure must repeat indefinitely as long as the timer is enabled.
5. To determine if a timeout event has occurred, monitor bit 7 of register 0x6D. To reset this event indicator, write a 1 to this bit (0x80). This is a convenience function. The software must provide the appropriate interrupt service routine etc. to respond to the timeout event if and when it occurs.
6. To disable the timer, clear bit 6 in register 0x68.

The detailed register information for the WDT is provided below. Register bits marked "-" are unused.

0x67 Write WDT Reload / Reset

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-

When the watchdog timer is enabled, the software must write to this register before the timer times out to prevent the selected timeout function from occurring. The value written does not matter.

When this register is written, the timer will reload to its original value and begin to count down again.

0x68 Write WDT Enable Register

Bit No.	7	6	5	4	3	2	1	0
Name	-	WDTEN	-	-	-	-	-	-

WDTEN Watchdog timer enable:

0 Disable WDT operation; timeout event will not occur.

1 Enable WDT operation; timeout event will occur if WDT is not retriggered before it times out.

0x69 Write WDT Timeout Event

Bit No.	7	6	5	4	3	2	1	0
Name	WDTEV3	WDTEV2	WDTEV1	WDTEV0	-	-	-	-

WDTEV3-0 Selects the event to occur upon timeout:

Binary	Hex	Signal / Function
0000	0	Invalid setting
0001	1	IRQ3
0010	2	IRQ4
0011	3	IRQ5
0100	4	IRQ6
0101	5	IRQ7
0110	6	IRQ9
0111	7	IRQ10
1000	8	Invalid setting
1001	9	IRQ12
1010	A	IRQ14
1011	B	IRQ15
1100	C	NMI Non-maskable interrupt
1101	D	System reset
1110	E	Invalid setting
1111	F	Invalid setting

0x6A Write WDT Timeout Interval Low Byte

Bit No.	7	6	5	4	3	2	1	0
Name	WDTD7	WDTD6	WDTD5	WDTD4	WDTD3	WDTD2	WDTD1	WDTD0

WDTD7-0 The lowest 8 bits of the 24-bit timeout interval

0x6B Write WDT Timeout Interval Middle Byte

Bit No.	7	6	5	4	3	2	1	0
Name	WDTD15	WDTD14	WDTD13	WDTD12	WDTD11	WDTD10	WDTD9	WDTD8

WDTD16-8 The middle 8 bits of the 24-bit timeout interval

0x6C Write WDT Timeout Interval High Byte

Bit No.	7	6	5	4	3	2	1	0
Name	WDTD23	WDTD22	WDTD21	WDTD20	WDTD19	WDTD18	WDTD17	WDTD16

WDTD23-16 The highest 8 bits of the 24-bit timeout interval

0x6D Write/Read WDT Timeout Indicator

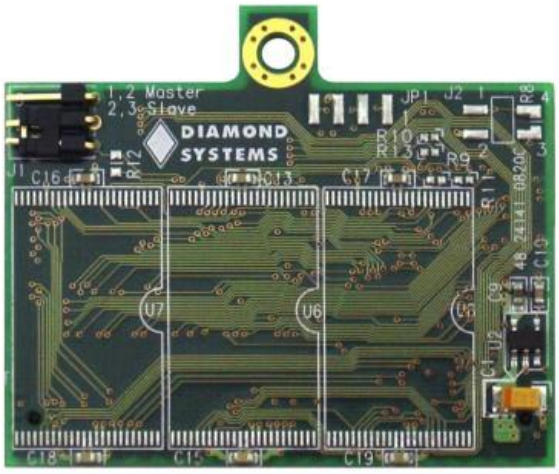
Bit No.	7	6	5	4	3	2	1	0
Name	WDTTO	-	-	-	-	-	-	-

WDTTO When this bit is 1, a timeout occurred on the watchdog timer. Write a 1 to this bit to reset the timeout indicator.

24. FLASHDISK MODULE

24.1 Overview

Helios is designed to accommodate an optional wide-temperature solid-state IDE FlashDisk module for rugged mass storage in place of a notebook hard drive or commercial flashdisk. This module contains 128MB to 4GB of solid-state non-volatile memory that operates like an IDE drive without requiring additional driver software support. It features automatic wear leveling and 1,000,000 write cycles minimum.



IDE Flashdisk (top side view; IDE connector is underneath)

24.2 IDE Flashdisk Models and Capacities

Model	*Capacity*
FD-128R-XT	128MB
FD-256R-XT	256MB
FD-512R-XT	512MB
FD-1GR-XT	1GB
FD-2GR-XT	2GB
FD-4GR-XT	4GB

24.3 Configuration and Installation

The flashdisk module contains a jumper block J1 for master/slave configuration. For master mode, install the jumper over pins 1 and 2. For slave mode, install the jumper over pins 2 and 3. The photo above shows Master mode (pin 1 is the lower pin near C16 / R12).

The flashdisk can also be configured for write protection. To write-protect the full disk, solder an 0603 or 0805 size 0-ohm resistor across pads 3-4 of jumper block J2 on the right side of the board (indicated as **R8** on the silkscreen). With the resistor in place, the files can still be read, but the disk cannot be written or erased.

The flashdisk module installs directly on the IDE connector, J12, and is held down with a spacer and two screws a mounting hole on the board. The mounting hardware is included with the flashdisk in hardware kit 6801008. The Helios SBC may already include the mounting spacer, in which case only the top side screw is required.

24.4 BIOS FlashDisk Configuration

To configure the Helios SBC to work with the flashdisk module, enter the BIOS by pressing **DEL** during startup. Select the Main menu, and then select *IDE Primary Master*. Enter the settings shown in the following table. Exit the BIOS and save the change. The system will now boot and recognize the flashdisk module as drive C:.

Setting	***128MB***	***256MB***	***512MB***	***1GB***	***2GB***	***4GB***
Type	User					
Cylinders	977	980	993	1986	3969	7937
Heads	8	16	16	16	16	16
Sectors	32	32	63	63	63	63
Multi Sector Transfer	Disable					
LBA Mode Control	Enable					
32 Bit I/O	Disable					
Transfer Mode	Fast PIO 1					
Ultra DMA Mode	Disable					

24.5 Using the FlashDisk with Another IDE Drive

The flashdisk occupies the board's 44-pin IDE connector and does not provide a pass-through connector. To utilize both the flashdisk and a notebook drive, the Diamond ACC-IDEEXT adapter is required, along with 44-wire cable number 6981004. The 44-wire cable carries power from the SBC to the adapter board and powers the flashdisk module and any drive using a 44-pin connector, such as a notebook hard drive.

A drive utilizing a 40-pin connector, such as a CD-ROM or full-size hard drive, requires an external power source through an additional cable. The power may be provided from the SBC's power out connector, J5, or from one of the two 4-pin headers on the ACC-IDEEXT board. Diamond Systems' cable number 6981006 may be used with either power connector to bring power to the drive.

25. MASS STORAGE ACCESSORIES

25.1 ACC-IDEEXT FlashDisk Programmer Board

The FlashDisk Programmer Board, model number ACC-IDEEXT, may be used to connect both a flashdisk module and a standard IDE hard drive or CD-ROM drive to the Helios SBC to allow file transfers to/from the flashdisk during system setup. The board can also be used to connect a flashdisk to a desktop computer to transfer files to the flashdisk.

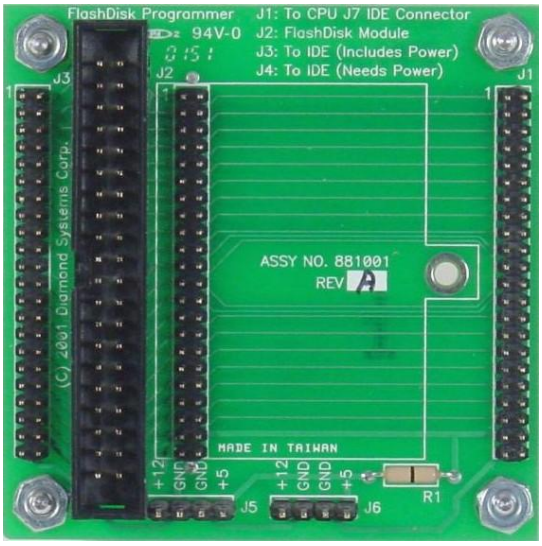
The ACC-IDEEXT comes with a 44-wire cable no. (DSC number 6981004) and a 40-wire cable no. (DSC number C-40-18) for connection to external drives. The flashdisk module is sold separately.

Both 40-pin .1-inch spacing and 44-pin 2mm spacing pin headers are provided on ACC-IDEEXT for connection to the flashdisk and a hard drive or CD-ROM drive. A dedicated connector, J2, is provided for the flashdisk module. It also provides a flashdisk mounting hole for permanent installations. The IDE cable, DSC nnumber 6981004, is normally used to connect the board to the SBC using one of the other 44-pin connectors. Any two devices may be connected simultaneously using this board with proper master/slave jumper configurations on the devices.

To connect a flashdisk + IDE notebook hard drive to the Helios, connect one end of cable 6981004 to the SBC, and attach the other two connectors to the ACC-IDEEXT and the hard drive.

To connect a flashdisk and CD-ROM to Helios, connect one end of cable 6981004 to the SBC and the other end to ACC-IDEEXT, and connect the C-40-18 (or a standard desktop IDE cable) from the 40-pin connector on ACC-IDEEXT to the CD-ROM. Power needs to be provided to the CD-ROM separately. The two 4-pin connectors J5 and J6 provide +5V power from the 44-pin cable and are compatible with a standard floppy drive connector. Note carefully the voltage indicators on the connectors. Red on the floppy drive cable is +5V and yellow is +12V. +12V is not present on the 44-pin connector or the ACC-IDEEXT.

To attach the ACC-IDEEXT to a desktop computer, attach the desktop 40-pin IDE cable to the 40-pin connector on the board and then provide power to J5 or J6 using the PC hard drive / floppy drive power cable. Note carefully the voltage indicators on the connectors. Red on the floppy drive cable is +5V and yellow is +12V. +12V is not present on the 44-pin connector or the ACC-IDEEXT and is not needed for operation.

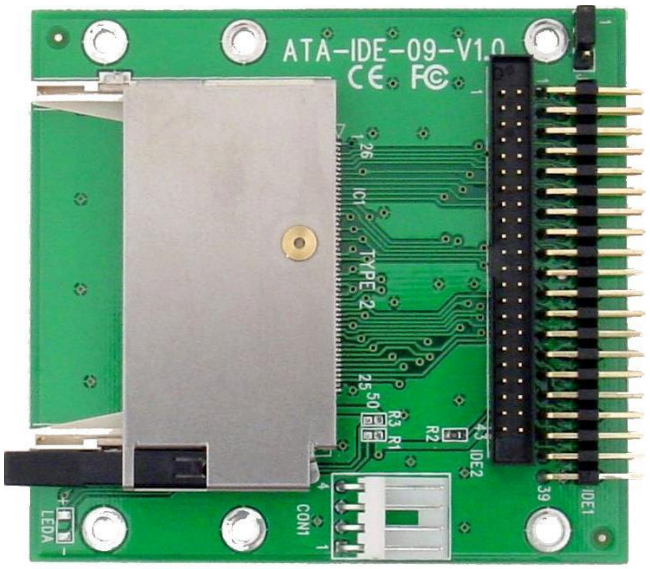


ACC-IDEEXT FlashDisk Programmer Board

25.2 ACC-CFEXT CompactFlash Adapter

The CompactFlash adapter, model number ACC-CFEXT, enables the use of a CompactFlash device for mass storage on the Helios SBC. It includes a 44-wire cable, part number 6981004. This cable connects from the IDE connector on Helios to the 44-pin connector on the adapter. Both IDE signals and +5V are provided to the board via the 44-wire cable.

The adapter may also be attached to a desktop PC for file transfer to the CF device. To do this, attach the desktop 40-pin IDE cable to the 40-pin connector on the ACC-CFEXT, and then provide power to connector CON1 using the PC hard drive / floppy drive power cable. Pin 1 of CON1 is +5V. +12V is not present on the 44-pin connector or the ACC-CFEXT and is not needed for operation.



ACC-CFEXT CompactFlash Adapter

26. PANEL I/O BOARD

The Helios Panel I/O Board, model PNL-HLV-02, provides a convenient way to access most of the SBC's I/O features without the use of cables. The bottom side contains 2mm female sockets on the bottom side that plug on top of the SBC and convert the SBC I/O pin headers to industry-standard connectors on the top side. Available I/O includes:

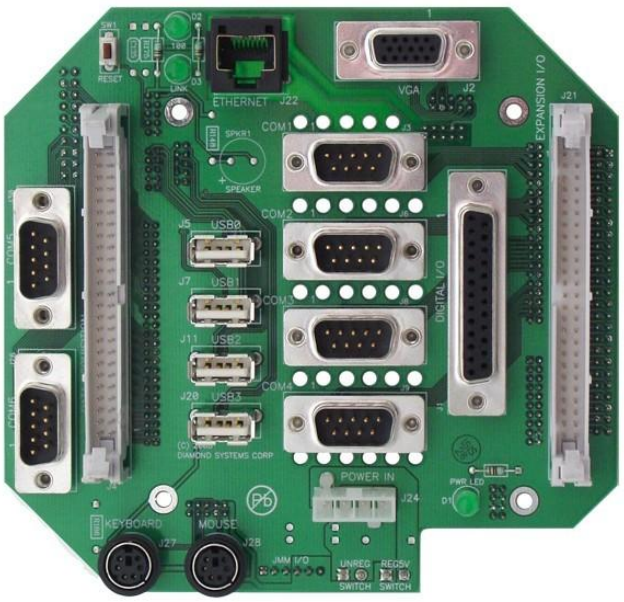
- 4 serial ports
- 4 USB ports
- VGA
- Ethernet
- Keyboard & mouse
- 16 digital I/O from Vortex CPU
- Data acquisition from Helios model HLV800-256AV

The panel I/O board may be used together with the Helios SBC in an "open frame" configuration, or the assembly can be installed in a Pandora enclosure to create a complete, cable-free, compact industrial computer. Pandora is available in multiple lengths to allow the installation of PC/104 add-on modules below the Helios SBC to provide additional functionality in the system.

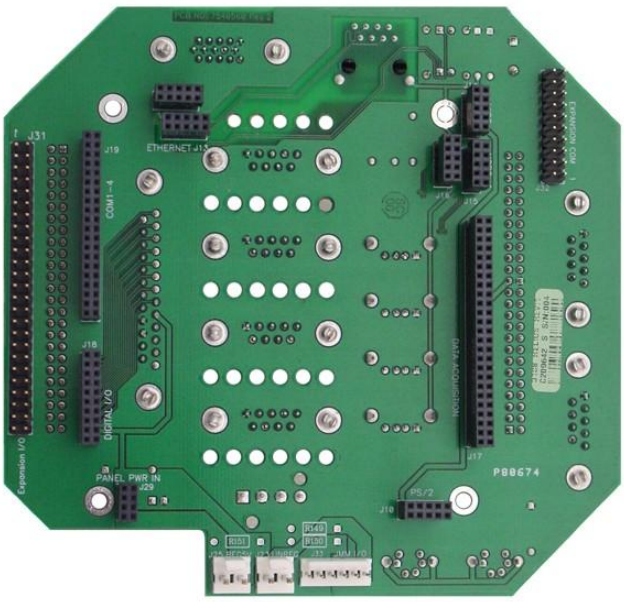
The PNL-HLV-02 includes two built-in expansion options to enable the use of additional boards inside the enclosure without requiring customization of the enclosure front panel or panel board. Additional boards are installed below the Helios SBC using the stacking PC/104 connector:

- A 50-pin latching connector enables access to one additional I/O board inside the enclosure. A 50-pin header on the bottom of the board is used to bring out the I/O from the installed PC/104 board with a ribbon cable. Any I/O board with a 50-pin connector can be easily attached, or a custom cable can be made to mate the I/O board's connector to the 50-pin header on the panel board.
- Two DB9M connectors on the front panel enable the use of 2 additional serial ports, for a total of 6. The additional serial ports are provided by installing a Diamond Systems' EMM-4M-XT board. A 20-pin connector on the bottom of the panel board is used to bring out the serial ports with a 20-pin ribbon cable.

In the photo at left, the 50-pin connector on the far right and the two DB9M connectors on the far left are the user-accessible expansion connectors. In the photo at right, the 50-pin header on the far left and the 20-pin header in the upper right are the internal connections for the add-on modules.



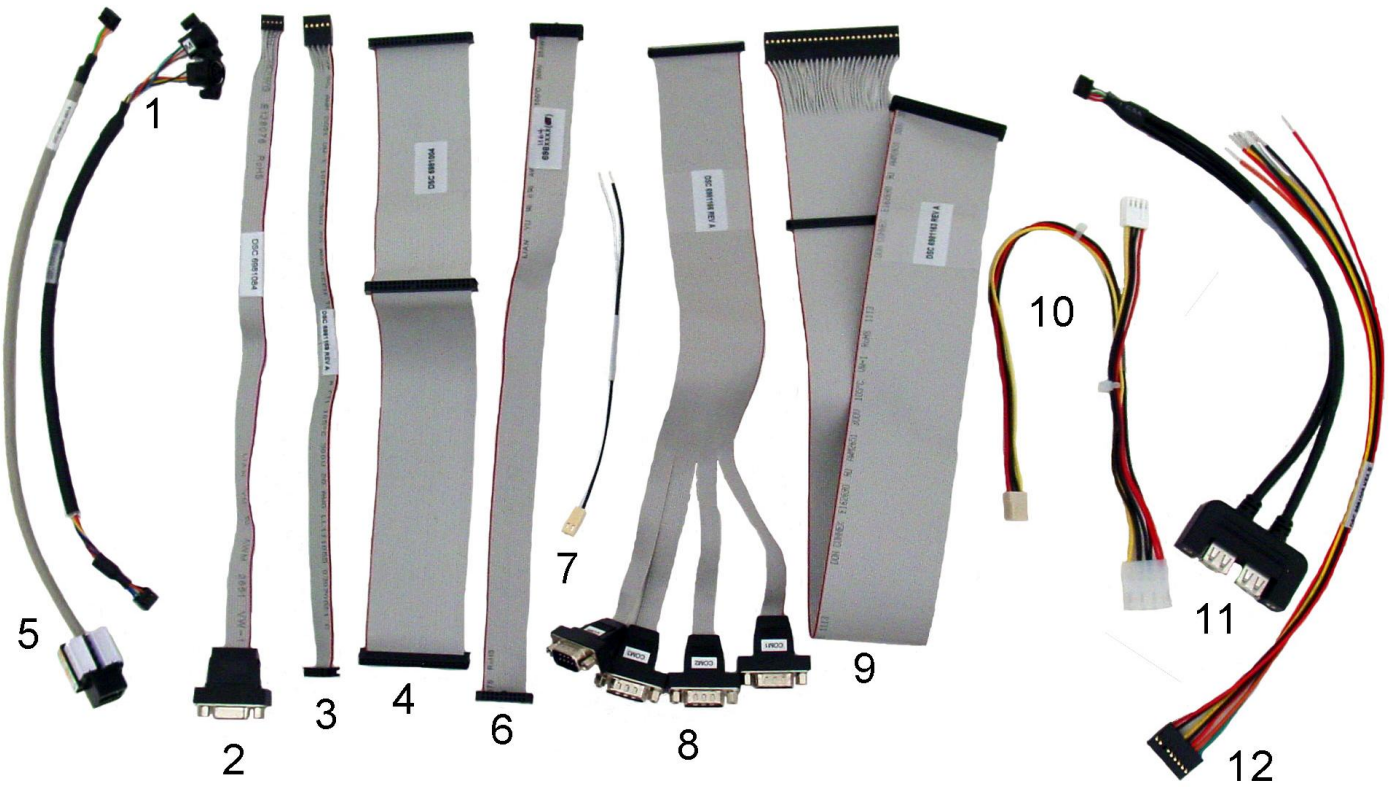
Helios Panel I/O Board, User Side



Helios Panel I/O Board, SBC Side

27. I/O CABLES

Diamond Systems offers Cable Kit C-HLV-KIT with cables for all I/O connectors on the board except the LCD and backlight. Some cables are also available separately.



Helios Cables Kit C-HLV-KIT

Photo No.	*Cable Part No.*	*Description*	*Helios Connector*
1	6981083	Keyboard/Mouse	J3
2	6981084	VGA	J10
3	6981169	Auxiliary	J14
4	6981004	HDD, IDE	J12
5	6981161	Ethernet RJ45	J11
6	6981164	Digital I/O	J7
7	6981180	External Battery	J6
8	6981166	Serial Ports 1-4	J8
9	6981163	Data Acquisition	J17
10	6981006	Power Out	J5
11	6981082	Dual USB (2 per kit)	J15, J16
12	6981009	Power In	J4

28. SPECIFICATIONS

28.1 Processor Section (All Models)

Item * means same as previous column	*HLV800-256DV / HLV1000-256V*	*HLV800-256AV / HLV1000-256AV*
CPU Circuit		
Processor	Vortex86DX	*
Speed	1GHz or 800MHz	*
Cooling	Heat sink	*
System bus	100MHz	*
SDRAM memory	256MB 533MHz DDR2, soldered	*
Display type	CRT 18-bit single-channel LVDS LCD	*
CRT resolution	1600 x 1200 max	*
LCD resolution	1600 x 1200 max	*
Video memory	128MB	*
USB ports	4 USB 2.0	*
Serial ports	COM1-2: 2 RS-232/422/485 COM3-4: 2 RS-232 fixed	*
Networking	10/100Mbps Ethernet integrated into Vortex processor	*
Mass storage	1 IDE channel with master/slave support IDE flashdisk interface	*
Keyboard/mouse	PS/2	*
Watchdog timer	24-bit counter 30.5us to 511 sec programmable interval	*
Expansion bus	PC/104 16-bit ISA bus	*
Digital I/O: J7 Ports D/E		
Number of I/O lines	16	*
Input voltage	Low: 0V min, 0.8V max High: 2.0V min, 7.0V max	*
Input current	Low: -5.0uA max High: 1.0uA max	*
Output voltage	Low: 0.2V min, 0.55V max High: 2.0V min, 3.3V max	*
Output current	Low: 64mA max at 0.55V High: 32mA max at 2V	*
Mechanical/Environmental		
System input voltage	5VDC ±5%	*
Power consumption	4.3W typical	5.4W typical 7.3W maximum
Dimensions	3.550” W x 3.775” H PC/104 compliant	*
Weight	2.5oz / 71g	3.1oz / 88g
MTBF		65,535 hours
Operating temperature	-40ºC to +85ºC / -40ºC to +71ºC	*
RoHS	Compliant	*

28.2 Data Acquisition Section (HLV800-256AV & HLV1000-256AV Only)

Analog Inputs	
Number of input channels	16 single-ended or 8 differential voltage inputs (software selectable)
Resolution	16 bits (1/65,536 of full scale)
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1.25V Unipolar: 0-10V, 0-5V, 0-2.5V, 0-1.25V
Input bias current	50nA max
Maximum input voltage	±10V for linear operation
Over-voltage protection	±35V on any input without damage
Drift	±10ppm/°C typical
A/D conversion rate	250,000 samples/second maximum
Conversion trigger	Software trigger Internal pacer clock External digital signal
FIFO	2048 samples Programmable interrupt threshold

Analog Outputs	
Number of output channels	8 voltage outputs
D/A resolution	12 bits (1/4096 of full scale)
Output ranges	Unipolar: 0-10V, 0-5V Bipolar: ±10V, ±5V, ±2.5V
Output current	±5mA max per channel
Settling time	4µS max to ±1/2 LSB
Relative accuracy	±1 LSB channel to channel
Nonlinearity	±1 LSB, monotonic

Digital I/O	**J17 Ports A, B, C**	**J17 EXTTRIG, TOUT1**
Number of I/O lines	24	2
Compatibility	3.3V and 5V logic levels	3.3V and 5V logic levels
Input voltage	Low: 0V min, 0.8V max High: 2.0V min, 4.25V max	Low: -0.3V min, 1.34V max High: 1.74V min, 4.25V max
Input current	+/-10µA max	+/-1µA max
Output voltage	Low: 0.0V min, 0.4V max High: 2.9V min, 3.3V max	Low: 0.0V min, 0.7V max High: 2.2V min, 3.1V max
Output current	Low: 12mA max High: -12mA max	Low: 8mA max High: -8mA max

Counter/Timers	
A/D pacer clock	24 bit down counter 10MHz, 1MHz, or external clock input
General purpose	16-bit down counter 10MHz, 100KHz, or external clock input